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Technical roadmap of ultra-thin crystalline silicon-based bioelectronics

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Technical roadmap of ultra-thin crystalline silicon-based bioelectronics

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Abstract

Ultra-thin Crystalline silicon stands as a cornerstone material in the foundation of modern micro and nano electronics. Despite the proliferation of various materials including oxide-based, polymer-based, carbon-based, and two-dimensional (2D) materials, crystal silicon continues to maintain its stronghold, owing to its superior functionality, scalability, stability, reliability, and uniformity. Nonetheless, the inherent rigidity of the bulk silicon leads to incompatibility with soft tissues, hindering the utilization amid biomedical applications. Because of such issues, decades of research have enabled successful utilization of various techniques to precisely control the thickness and morphology of silicon layers at the scale of several nanometres. This review provides a comprehensive exploration on the features of ultra-thin single crystalline silicon as a semiconducting material, and its role especially among the frontier of advanced bioelectronics. Key processes that enable the transition of rigid silicon to flexible form factors are exhibited, in accordance with their chronological sequence. The inspected stages span both prior and subsequent to transferring the silicon membrane, categorized respectively as on-wafer manufacturing and rigid-to-soft integration. Extensive guidelines to unlock the full potential of flexible electronics are provided through ordered analysis of each manufacturing procedure, the latest findings of biomedical applications, along with practical perspectives for researchers and manufacturers.

Keywords: crystalline silicon, oxidation, doping, transfer process, flexible bioelectronics

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1. Introduction

Bioelectronics is rapidly emerging as a transformative field, sitting at the intersection of biology and electronics, with immense potential for advancing medical diagnostics, therapeutic interventions, and biological interfacing[1–16]. This interdisciplinary approach allows for the development of sophisticated devices that seamlessly interact with the natural processes of the human body, offering real-time monitoring and precise therapeutic delivery. However, the success of these devices hinges on the careful selection of materials that must meet rigorous criteria, such as exceptional electrical properties, mechanical flexibility, biocompatibility, and in certain cases, biodegradability. The challenge lies in finding materials that excel across these domains, as strengths in one area may come at the expense of another[17–21]. For instance, materials such as copper, known for their high electrical conductivity, may not be biocompatible[22–23], while others such as polydimethylsiloxane (PDMS), valued for its flexibility, might not be capable of enduring the body's internal environment[24].

Among the various options, semiconducting materials are particularly crucial for bioelectronics due to their roles in sensing, actuation, and logic operation[25–31]. Organic semiconductors have been explored for their intrinsic flexibility and ease of fabrication. However, their limited electrical performance and chemical stability pose challenges for high-performance bioelectronics. Inorganic semiconductors, including metal oxides, III-V compound semiconductors, 2D materials, and silicon, generally provide superior electrical properties. III-V compound semiconductors, such as gallium arsenide (GaAs), offer excellent electrical performance due to their high electron mobility and direct bandgap, which enable fast electronic and optoelectronic responses. However, III-V compound semiconductors require high-vacuum equipment such as molecular beam epitaxy (MBE) or metal-organic chemical vapor deposition (MOCVD) for fabrication, significantly increasing production costs. Additionally, during epitaxial growth, lattice mismatch between the substrate and III-V layers can lead to misfit dislocations and other crystal defects, degrading device performance. These challenges, combined with the high cost of III-V materials, make large-area fabrication difficult. Furthermore, the need for precise vacuum equipment and the issues of lattice mismatch during epitaxy further exacerbate the challenges of large-scale production[32–36]. Similarly, 2D materials, like graphene, exhibit remarkable electrical properties, including high conductivity and carrier mobility, attributed to their unique atomic-scale thickness and crystal structures that minimize the scattering of charge carriers. However, despite these advantages, 2D materials face significant challenges in scalability and uniformity, making it difficult to integrate them into conventional manufacturing processes, particularly for large-area fabrication[37–41]. Metal oxides offer another option for bioelectronics, as they can be processed at low temperatures, which is advantageous for flexible and stretchable device manufacturing[42–48]. Metal oxides such as zinc oxide (ZnO) and titanium dioxide (TiO_2) are widely used due to their good semiconducting properties, chemical stability, and ability to function as both conductors and insulators depending on their composition. However, metal oxides tend to suffer from reliability issues during operation, especially under mechanical stress. Liquid metal oxides, such as gallium-based alloys, offer advantages like self-healing and maintaining conductivity under deformation but face issues like oxidation and leakage, limiting device stability[49–56]. Nanomaterials, such as carbon nanotubes and quantum dots, further expand the possibilities for bioelectronics with their exceptional mechanical flexibility and tunable electronic properties, making them ideal for flexible and stretchable electronics[57–65]. However, their integration into devices often encounters significant manufacturing hurdles, including poor scalability and batch-to-batch variability, which result in inconsistent performance and limited feasibility for large-scale production. Additionally, the relatively low electron mobility of these materials compared to silicon and III-V compound semiconductors restricts their performance in high-speed or high-frequency applications. Although the flexibility of inorganic materials can be improved through thinning processes, they still face significant integration challenges. III-V compound semiconductors, 2D materials, and metal oxides often struggle to integrate into conventional manufacturing processes while maintaining both performance and durability, particularly when scaling up for large-area fabrication. These constraints severely limit their broader application in bioelectronics[46–47, 66–71].

Compared to silicon, which offers superior electrical performance, mature fabrication processes, and proven long-term stability, these emerging materials frequently fall short in achieving the same level of reliability and precision required for high-performance bioelectronic applications.

These limitations highlight the importance of a synergistic approach that combines the strengths of silicon with the unique properties of alternative materials. By leveraging silicon as a reliable foundation, alongside the complementary advantages of materials like metal oxides and nanomaterials, it is possible to drive innovation in bioelectronics and develop robust, scalable solutions for next-generation devices.

Crystalline silicon stands out due to its balanced combination of high electrical performance, chemical stability, and mature manufacturing processes. It integrates seamlessly into established fabrication methods, such as complementary metal oxide semiconductor (CMOS) technology, making it widely available and cost-effective. Additionally, crystalline silicon can be reliably thinned to achieve flexibility without compromising its inherent stability, ensuring long-term functionality in bioelectronic devices. Recognized for its exceptional electronic properties, including high carrier mobility and reliable thermal/mechanical stability, silicon has long been a cornerstone of the semiconductor industry. Its compatibility with CMOS technology ensures its continued relevance in modern electronics, and advanced processes like doping, etching, and nanoscale patterning allow for precise control over its properties, driving innovation in applications ranging from computing to energy solutions. This combination of robustness, adaptability, and ease of integration makes crystalline silicon indispensable for bioelectronic applications, avoiding many of the challenges associated with other inorganic semiconductors[72–95].

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As shown in **Figure 1**, the evolution of silicon as a transformative material began in the mid-20th century, revolutionizing electronics with its pivotal role in the creation of transistors and integrated circuits[96]. These early advancements laid the groundwork for modern computing. During the 1950s and 1960s, silicon's adoption in semiconductors rapidly expanded due to its excellent electrical properties, abundant availability, and ease of doping, establishing it as the backbone of the electronics industry[97–100]. The 1970s and 1980s further reinforced the importance of silicon with the advent of microelectronics, driving the development of more compact and powerful computing devices[101–104]. The 1990s marked a significant leap in silicon technology with the introduction of thin-film processes, particularly for flexible solar cells, which demonstrated silicon's ability to maintain high electronic performance while being physically flexible[105]. This capability was crucial for the development of flexible electronics, including bioelectronic devices, where silicon's properties needed to be retained even when applied to irregular biological surfaces. The early 2000s brought about the development of transfer techniques, enabling the precise integration of silicon with various substrates, such as soft and biocompatible polymers, paving the way for flexible, high-performance bioelectronic devices[92, 106–108].

In bioelectronics, the journey of crystalline silicon began with its application in flexible solar cells, highlighting its capability to combine high electronic performance with flexibility[81, 109–124]. This success prompted researchers to explore its use in bioelectronics, where the ability of silicon to conform to the natural contours of biological surfaces became particularly valuable. One of the key advantages of silicon is its mechanical flexibility, which, when coupled with its excellent electrical properties, makes it ideal for developing wearable sensors and implantable devices, such as e-skin and body-adherent electronics. Furthermore, utilizing various encapsulation methods alongside the biocompatibility of silicon and the discovery of its biodegradability in biological environments opened up new possibilities for transient electronics-devices designed to dissolve within the body after serving their purpose, such as temporary medical implants and drug delivery systems[125–126]. This advancement represents a significant leap forward in bioelectronics, reducing long-term risks associated with permanent implants and enabling novel bio-integrated applications. Silicon has demonstrated its versatility not only in single devices but also in complex bioelectronic systems, including artificial sensory systems inspired by natural or human biological systems[127–131]. Today, silicon stands at the forefront of bioelectronics, leveraging its unique properties-biocompatibility, biodegradability, and nanoscale precision to develop innovative devices that interact with the human body in unprecedented manners. As research continues, the portion of silicon in the realm of bioelectronics is foreseen to expand, solidifying its position as a core material in the development of future medical technologies and next-generation flexible electronics.

As depicted in the innermost hexagon of **Figure 2**, the application of crystalline silicon in bioelectronics requires a multidisciplinary engineering approach, integrating principles from electrical, mechanical, optical, and materials engineering, as well as biotechnology. This interdisciplinary collaboration is essential for addressing the complex and multifaced challenges of integrating silicon with biological systems[132–133]. For instance, while electrical engineering focuses on optimizing the electrical conductivity and electronic properties of silicon, mechanical engineering ensures the flexibility and durability under dynamic biological environments. Optical engineering contributes to obtaining a quality optical interface, meantime material engineering addresses the compatibility of silicon with various foreign matters. Biotechnology plays a crucial role in ensuring that the engineered silicon interfaces safely and effectively with biological tissues, maintaining biocompatibility throughout the entire device lifecycle.

After such multidisciplinary collaboration for setting up the system as a whole, the focus must now shift to developing practical strategies for device fabrication. Transforming rigid crystalline silicon into flexible components for bioelectronic devices involves advanced manufacturing schemes, including thin-film processing and various transfer techniques[134–139]. As portrayed in the rainbow-hued circular layer of **Figure 2**, the strategies for obtaining such flexible devices can be broadly illuminated in two distinct approaches. The procedure described in clockwise direction demonstrates the general process of substrate transfer, in which a layer of ultrathin silicon is transferred onto flexible substrates, followed by a series of flexible fabricating processes to complete the device. On the other hand, the counter-clockwise sequence contains steps of initially completing the fabrication of the device on a rigid handling wafer, followed by bonding a layer of foreign material that will serve as a flexible substrate, and finalized by removing the handling wafer via back-etching to release the device in its flexible morphology. Both methods involve precise silicon manufacturing to retain the excellent electronic properties while imparting the required flexibility for bioelectronic applications.

Devices produced with such an extremely thin profile are appointed the capability to accommodate complex biological surfaces, rendering them suitable for various biomedical applications. Six representative bio-integrated applications utilizing the bioelectronic devices, obtained through such rigorous processes, are illustrated in the outermost segmented regions and graphics of **Figure 2**. Such applications encompass using the fabricated device for: mechanical monitoring, biochemical monitoring, active device, optoelectronic stimulation, thermal detecting, and electrophysiological recording. Based on its compatibility with mature CMOS technology, the versatile ability to alter the physical form and material property of silicon is ever expanding the employment of silicon-based flexible electronics. As technology continues to advance, crystalline silicon is poised to play an increasingly important role among the future of bioelectronics, offering unprecedented opportunities for innovation in medical diagnostics, therapeutic interventions, and so beyond.

In this review, we aim to comprehensively explore the processes, characteristics, applications, and challenges

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necessary to fully harness the potential of crystalline silicon in bioelectronics. We delve into the intricate processes involved with transforming rigid crystalline silicon into flexible frameworks suitable for various bioelectronic applications. Starting with on-wafer manufacturing and subsequently being classified into substrate transfer processing and device transfer processing, we follow the trajectory of contemporary manufacturing strategies of silicon-based flexible devices. Additionally, we highlight real-world biomedical applications of silicon-based electronics and discuss the innovative characteristics that enable such versatile employments. Our review is expected to serve as an organized blueprint by presenting practical guidelines for silicon manufacturers, integrating both scholarly foundations and experiential perspectives.

2. On-wafer manufacturing

To leverage the exceptional properties of single crystalline silicon in flexible bioelectronics, it is essential to develop manufacturing strategies that embrace the physical and chemical constraints brought up within the entire processing sequence[72]. The inherent limitations of the materials involved in each stage determine the order or occasionally prohibit the utilization of certain manufacturing steps altogether[42, 140].

One critical consideration is the temperature at which the sample is subject to during the manufacturing process[141–142]. Ultra-thin silicon components transferred onto flexible substrates stand strong as a core element of silicon-based flexible electronics[143–144]. However, the low thermal budget of such foreign substrates poses a significant challenge, as it renders them incompatible with high-temperature silicon processes[145]. Typical high-temperature processes include oxidation and doping, which are instrumental in precisely modulating the material property of silicon[146]. These processes, as a part of the eminent CMOS technology, have been fundamental to establishing silicon as the backbone of the modern micro and nano electronics industry[145]. Nonetheless, in the context of flexible electronics, the low thermal tolerance of substrates necessitates that such processes be completed prior to transfer printing, thereby constraining their utilization[147–149].

Through the following section, we examine such procedures that are suitable of being carried out during the on-wafer phase among the whole manufacturing cycle. Particularly, due to the high-temperature conditions involved in each process, oxidation and doping are categorized as the on-wafer manufacturing processes, and practical guidelines are provided by discussing their fundamental principles, applications, and some heuristic considerations that researchers must keep in mind to ensure successful implementations.

2.1 Oxidation

The thermally grown silicon dioxide (t-SiO_2) formed on silicon wafers grows according to the Deal-Grove (DG) model[150–153], which describes the oxidation process through a combination of surface reaction kinetics and diffusion of oxidizing species through the growing oxide layer, as shown in **Figure 3(a)** and **(b)**. Examining the oxide thickness and oxidation time, the DG model accurately describes the relationship between these two parameters when the oxide thickness is greater than 23 nm[154], whereas different analytical methods and models are applied in situations with thinner oxide thicknesses[151, 154–157].

Due to its excellent insulating properties[158–162], high thermal stability[163–166], structural uniformity[160–161, 167–168], quality Si/SiO_2 interface[169–170], and minimal defect density[159, 161–162, 165, 167–168, 171–172], t-SiO_2 exhibits superior performance in various applications and has been widely utilized in flexible electronics[173–174]. The growth of t-SiO_2 requires high-temperature thermal processing in a tube furnace at elevated temperatures, typically around 1 000 °C[175–176]. However, a challenge arises as flexible substrates generally have low thermal budgets, rendering them incompatible with such high-temperature processing steps[146, 175, 177–183]. As a result, the growth and application of t-SiO_2 layers are restricted to the on-wafer manufacturing phase, prior to transferring the sample onto thermally unbearable substrates[44, 174, 183–185].

During the manufacturing process of silicon-based flexible bioelectronics, t-SiO_2 may be utilized for various purposes, such as for silicon thinning, or as a hard mask during etching or doping [176] of the underlying silicon layer. Among these given applications, t-SiO_2 is employed in a rather transient form; of which the oxide layer temporarily appears during the manufacturing process to perform the necessary function and is removed afterwards. This contrasts with the usage of t-SiO_2 in a permanent form, where the oxide layer remains within the composition of the final device to perform specific functions[173]. The transient use of t-SiO_2 primarily appears in the early stages of manufacturing and is employed for modulating the properties of silicon, which justifies its classification under the on-wafer manufacturing process, as depicted throughout Section 2.1. On the other hand, considering the characteristics and sequential order of the processing steps, which is typically achieved through back-etching and layer transferring[166, 174, 186–187], the permanent usages of t-SiO_2 will be addressed in the subsequent sections of this article.

As a starting point, thermal oxidation can be employed as a method to control the thickness of silicon layers[188], which is commonly referred to as 'silicon thinning'[75]. Unlike deposited layers of silicon dioxide, where the oxide layer is newly formed on the surface of the target samples, thermal oxidation grows an oxide layer on the silicon surface by consuming a certain amount of the mother wafer[189–190]. The thickness ratio of consumed silicon to newly formed t-SiO_2 layers adheres to a quantitative ratio of 0.44:1. In other words, when a t-SiO_2 layer with the tox (thickness of oxide layer) is grown, the amount of oxide that is created below the original wafer surface is 0.44 tox, while the amount formed above the surface is 0.56 tox as shown with dashed lines of **Figure 3(a)**. Silicon thinning through thermal oxidation utilizes this fact to attain precise thickness control of the silicon membrane, prior to its release, during the on-wafer processing stage. **Figure 3(c)** illustrates the generic process of using thermal oxidation for silicon thinning. The process is

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performed by repeating thermal oxidation and removal of the oxide layer formed thereby. Thickness modulation via thermal oxidation can be controlled at the nanometre scale by adjusting parameters such as the oxidation time or the processing temperature[188]. Furthermore, due to the excellent selective etching of SiO_2 over Si with HF[191–193], with a substantial body of literature addressing the physics of thermal oxidation[194–195], the process can be conducted repeatedly until the desired thickness is achieved[196–199].

Silicon membranes obtained with nanometre-scale thicknesses exhibit varying properties depending on their physical dimensions[93, 200–201]. Existing research demonstrates the differing mechanical, electrical, chemical, optical, morphological, and biodegrading properties of silicon membranes with varying thicknesses[170, 199, 202–203].

Figure 3(d) highlights the performance variation of a wearable NO/NO_2 gas sensing system using silicon nano-membrane (SiNM) of different thicknesses, with the optimal SiNM thickness being determined through silicon thinning with thermal oxidation. The authors conduct repeated thermal oxidation of a silicon-on-insulator (SOI) wafer at a high-temperature of 1 100 °C and removal of the grown t-SiO_2 layer with HF, to achieve the expected thickness of SiNMs. As depicted in **Figure 3(e)**, the 100 nm thick SiNM used in the sensor exhibited about 20 times higher sensitivity and nearly 10 times greater recovering ability about 9.41 μg L^{-1} of NO_2 at room temperature, when compared to SiNMs with the thickness of 50 nm and 200 nm, respectively[204]. The highest sensitivity was observed with the 50 nm thick SiNM, which can be attributed to its exceptionally high surface-to-volume ratio. This enhanced ratio increased the active surface area available for gas adsorption, allowing for more efficient charge transfer interactions between the NO_2 molecules and the SiNM surface.

Owing to the forming mechanism of the oxide layer, silicon thinning is achievable exclusively through thermal oxidation, rather than other oxidation methods[205]. The ability to meticulously optimize device components by introducing physical variations through such highly reliable CMOS-compatible silicon processing is of great advantage in the field of modern bioelectronics[206–210]. After reaching the desired thickness, the t-SiO_2 layer is completely removed, exposing the underlying silicon layer for subsequent processing. As part of the on-wafer manufacturing process, its distinctive procedural characteristics allot silicon thinning as a transient usage of t-SiO_2.

Another form of the transient usage of t-SiO_2 layers is their application as masking layers. Among the manufacturing process of flexible electronics, hard masks are essential for defining necessary regions during the steps of etching and doping[211–214]. Due to its stability and superior oxide quality[215–216], t-SiO_2 can be utilized as such doping masks (**Figure 3(f)**, left) and etching masks (**Figure 3(j)**, left). The most common mask-formation procedure involves growing t-SiO_2 on the silicon surface through thermal oxidation, followed by photolithography to define patterned regions where the oxide is removed to expose the underlying silicon surfaces[217–218]. These exposed regions subsequently interact with reactants (in the case of etching masks) or dopants (in the case of doping masks) throughout the following fabrication steps, resulting in altered properties of the subject locales.

The use of t-SiO_2 as an etching mask is based on its excellent physical stability and the significant etching selectivity between SiO_2 and Si[219–220]. Selectivity in this context implies both the selectivity of reactants used during the etching process[221–222] and HF solution used post-etching to remove the oxide masking layer[191–192]. Among a wide variety of silicon etchants that are used, SiO_2 shows the etching rate of 0.05–3 nm $\cdot$min^{-1} against tetramethylammonium hydroxide (TMAH) and 0.5–7.5 nm $\cdot$min^{-1} against potassium hydroxide (KOH), depending on the concentration and temperature of the etchant solution, each slower than the rate of silicon by several orders of magnitude (ranging in 80–1 000 nm $\cdot$min^{-1} and 300–1 500 nm /min^{-1}, respectively)[222–228]. Furthermore, the excellent physical stability of t-SiO_2 is attributed to its defect-free nature and lower porosity compared to deposited oxide[229–231]. This high-quality, dense oxide layer, both physically and chemically suitable for its use, can thus be effectively utilized as a reliable etching mask.

The common application of t-SiO_2 as an etching mask goes beyond its use as a hard mask during the reactive-ion etching (RIE) of the underlying silicon layer[224, 232–235]. It is also frequently used as a sidewall passivation layer [236] in the top-down approach for silicon manufacturing in flexible bioelectronics[237–238], particularly during the bulk Si wafer undercut process for SiNM/silicon nano-ribbon (SiNR) release[239]. By taking advantage of the fact that silicon in the [111] direction has an etching rate several orders of magnitude smaller than that in the [110] direction when exposed to TMAH and KOH[240–243], high-quality SiNM/SiNRs can be produced via anisotropic etching along trench patterns on the surface of bulk silicon wafers[244]. Since wet etchants will continue to anisotropically etch any silicon surface they encounter[73, 245], it is crucial to thoroughly cover the areas of silicon that are not meant to be modulated, ensuring they do not form an etching interface. In these processes, t-SiO_2 is employed to protect the silicon sidewalls from such reactants. As the aforementioned silicon thinning utilizes the substrate-consuming growth mechanism of thermal oxidation, sidewall passivation also stems from the intrinsic growth principle of t-SiO_2[88, 246]. Unlike deposited oxide, t-SiO_2 forms a uniform oxide layer among the surface in reaction with oxidants, resulting in a consistent oxide layer across all the exposed silicon surface[247–248]. Therefore, among applications that require passivation along the sidewalls of deep trenches, t-SiO_2 is considered far more suitable than deposited oxide[249–250].

Figure 3(f) depicts the generic flow of utilizing t-SiO_2 as a sidewall passivation layer during the formation of SiNRs using TMAH for wet anisotropic etching[251]. Starting on a bulk Si wafer, a trench is formed perpendicular to the [110] plane with its depth determining the final thickness of the SiNM/SiNR. After the trench formation, thermal oxidation grows a sidewall passivating t-SiO_2 layer along the trench exterior. For additional

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stability and protection, additional capping layers (typically SiN_x or metal) may be introduced[244]. After removing the passivation layer on the trench floor, further silicon etching is performed to create openings where wet etchants can penetrate to initiate anisotropic etching in the distinguished direction (e.g. in the direction of [110] for TMAH or KOH). The lateral dimension of undercut can be controlled by adjusting the sample immersion time in the etchant, until the silicon layer is released from the mother wafer and ready to be transferred onto a foreign substrate[144, 252]. Additionally, by precisely controlling the lateral dimensions of the undercut silicon or oxide layer or utilizing additional polymer layers, it is possible to create predefined structures, which serve as 'breakable anchors'[77, 253–256]. These anchors incorporate interlocking patterns, such as trench geometries and bracket-like terminations, which ensure mechanical stability during processing and allow for controlled detachment at the desired stage[140, 257]. Such designs are critical for preventing the released silicon membranes from floating away before the transferring process is initiated[258–260].

A Si_3N_4/t-SiO_2 bilayer was applied as sidewall passivation to protect against KOH etching during the formation of SiNRs on [111] bulk silicon wafers[252]. An additional Ti/Au metal mask was formed by angled (75 ° from the normal axis of the wafer) E-beam evaporation, exposing the Si_3N_4/t-SiO_2 bilayer at the bottom of the groove. The bilayer was subsequently removed to disclose the underlying silicon layer to create an interface for the undercut etching to occur. **Figure 3(g-i)** shows an scanning electron microscope (SEM) image of a sample right after the sidewall passivation was performed, demonstrating the conformal step coverage achieved through the Si_3N_3 deposition over the uniformly formed t-SiO_2. **Figure 3(g-ii)** exhibits the SiNRs formed as a result of anisotropic undercut etching along the [110] direction of the bulk wafer by KOH.

An ultrathin metal oxide semiconductor field-effect transistor (MOSFET) was formed on a bulk wafer and released using TMAH anisotropic etching[158]. After defining the source and drain regions through patterned doping and region definition, the authors grew a 50 nm thick t-SiO_2 layer through thermal oxidation at 1 100 °C for 17 minutes. In addition to serving as the gate dielectric, this t-SiO_2 layer acts as the sidewall passivation layer for the pre-defined trenches during the release process (**Figure 3(h)**, top). Along with depositing an additional SiN_x layer for better protection of the gate dielectric and the metal contacts, the sample was immersed in boiling TMAH solution for 90 minutes for wet anisotropic etching. As the exposed silicon (underlying silicon of which the passivation layer is removed by RIE) comes into contact with the TMAH solution, wet anisotropic undercut etching occurs along the [110] direction, causing the MOSFETs to be released from the mother wafer (**Figure 3(h)**, bottom). Due to the excellent thickness control capability of such top-down approaches, it is possible to release silicon structures in various geometries, including ribbons, bars, platelets, and membranes, with their thickness precisely controlled at nanometer scale. **Figure 3(i)** shows a set of SEM images of silicon membranes produced in this manner, with different thicknesses of 800 nm (top) and 11 μm (bottom).

Another application of the transient t-SiO_2 layer that we will examine is its usage as a doping mask, among the manufacturing process of Si-based flexible bioelectronics[77]. The methods for silicon doping broadly fall under two categories: diffusion and ion implantation[261–263]. The former relies on the substitutional/interstitial diffusion of impurities into the silicon crystal at high temperatures around 1 000 °C[264–265]. The latter involves a step of high-temperature annealing after the ion implantation, as well conducted around 1 000 °C, to repair the crystalline lattice damaged by high-energy ion implantation and activate the implanted ions[266–268]. These high-temperature processes restrict the standard usage of polymer or metal hard masks[269–273]. By utilizing thermal oxidation, a t-SiO_2 hard mask applicable to both diffusion and ion implantation can be obtained.

Taking advantage of the fact that the diffusion coefficient of impurities is larger in silicon compared to silicon oxide, t-SiO_2 can be used as a diffusion mask[274–275]. In addition, t-SiO_2 can be used as an ion implantation mask to physically separate the areas that require property modulation from those that do not, revealing only the areas that need to be doped[276]. However, during the high-temperature thermal annealing process that follows ion implantation, impurities may diffuse across the oxide layer and modulate the characteristics of the underlying silicon[277–279]. Therefore, it is advisable to remove the t-SiO_2 layer used as a doping mask before the subsequent thermal annealing process, in order to avoid the so called 'impurity diffusion' across the oxide layer[280].

Figure 3(j) shows the generic process of utilizing a t-SiO_2 layer as a doping mask. To prevent the involvement of unwanted defects during the oxidation and doping processes, the silicon wafer is meticulously cleaned before growing a high-quality t-SiO_2 layer on it[281–285]. Afterwards, doping patterns are engraved onto the oxide layer, typically by conventional photolithography, followed by the actual introduction of impurities among the exposed regions of silicon. By removing the masking layer through selective etching of t-SiO_2, a pattern doped silicon device is finally obtained.

As such highly reliable CMOS-compatible processes are involved[145], fine adjustment of the device doping profile and performance optimization accordingly becomes possible[286–288]. Huang *et al.* employed t-SiO_2 as a doping mask in the production of a SiNM-based positive-intrinsic-negative (PIN) diode for an epidermal radio frequency (RF) power harvester as a substitute of rigid batteries (**Figure 3(k)**)[289]. As shown in **Figure 3(l)**, a layer of t-SiO_2 on the top silicon of the SOI wafer has been used as a diffusion mask for both p-type doping using boron and n-type doping using phosphorus. **Figure 3(m)** is a colorized SEM image of the diode transferred onto a skin replica, to serve as a wearable power harvester. The researchers compared and optimized the device performance by varying the surface area of the doped regions on a scale of several hundred micro-meters (0.4, 0.15, 0.17 mm^2 for D1, D2, D3, respectively) while maintaining the length of the intrinsic region (7 μm) of the PIN diode. **Figure 3(n)** (left) shows three samples with different geometries. The ability to fabricate these patterns with such

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precision allowed the samples to be compared with simulation results to verify and optimize the overall performance of the system (right). The samples with different doping profiles were compared in terms of threshold voltage, current level, junction capacitance, and junction resistance to select the favorable design.

2.2 Doping

Along with the thermal oxidation of silicon, doping is another typical high-temperature process that must be performed during the on-wafer manufacturing phase[290]. Silicon doping is typically achieved through two methods: diffusion doping and ion implantation[291]. In diffusion doping, dopant atoms are introduced into the silicon lattice by exposing it to a high-temperature gaseous environment, allowing the dopants to diffuse into the substrate[292–293]. Ion implantation, on the other hand, involves bombarding the silicon surface with ionized dopants at high energy, followed by a thermal annealing process to repair the damaged crystal lattice and activate the dopants[263, 294–295]. For each method, high-temperature processing occurs during the diffusion phase or the post-implantation thermal annealing process, respectively[296].

Doping involves the deliberate introduction of impurities into the silicon lattice to manipulate the electron and hole concentrations in silicon[297]. The balanced state of electrons and holes is disturbed so that one of the two outnumbers the other, characterizing the silicon as an extrinsic semiconductor, in which the charge carrier concentration is inconsistent with the intrinsic carrier concentration in thermal equilibrium[298]. Regarding the doping of silicon, phosphorus and boron are some commonly used dopants for n-type and p-type doping[262, 299], respectively, due to their low ionization energy at room temperature[300–303].

As shown on the left of **Figure 4(a)**, a phosphorus atom introduced into the crystalline silicon lattice functions as a donor, contributing a free electron to the crystal lattice. Because phosphorus is a pentavalent element with five valence electrons, while silicon has four, the extra electron is left loosely bound to the phosphorus atom[290, 304]. Due to its low electron binding energy (0.045 eV), which is smaller than the average thermal atomic vibration energy of silicon (0.07 eV), the donor atom is easily ionized at room temperature, contributing a free electron to the conduction band[305]. These free electrons do not generate holes in the valence band and can move freely through the silicon crystal[306]. As a result, the silicon becomes a n-type semiconductor, characterized by a higher concentration of negatively charged electrons as the majority carriers. In contrast, as shown in the right of **Figure 4(a)**, the addition of a boron atom, a trivalent element with only three valence electrons, results in the formation of a vacancy, or 'hole', in the silicon crystal structure. With the relatively low binding energy (0.045 eV) of these holes to the boron atom, the hole can be easily freed at room temperature without any additional creation of electrons in the conduction band. Consequently, the silicon becomes a p-type semiconductor, distinguished by a higher concentration of positively charged holes as the majority charge carriers.

The introduction of such impurity atoms also results in shifting the Fermi energy level in the band energy diagram, as shown in the bottom row of **Figure 4(a)**[307–308]. In n-type doping, the Fermi level moves closer towards the conduction band as donor impurities increase the electron concentration, creating a condition of which $(E_C - E_F) < (E_F - E_V)$ is achieved. Conversely, in p-type doping, the Fermi level shifts closer towards the valence band, as the hole concentration is greatly enhanced by the acceptor impurities, making $(E_C - E_F) > (E_F - E_V)$[309–312]. The upward shift in n-type silicon reflects a higher likelihood of electron occupancy in the conduction band, whereas the downward shift in p-type silicon indicates a greater probability of hole occupancy in the valence band[313–314].

Such deliberate modulation of the electrical properties of silicon comes to serve as the cornerstone of modern CMOS technology[315–316]. Especially, owing to its capability to impart the desired level of electrical conductivity specifically to the pre-defined terrain of silicon, doping holds substantial importance among the variety of technologies[317–319]. One of the significant advantages of the mature CMOS fabrication process is its ability to achieve high-density integration[320–321], making it suitable for various applications among fields ranging from consumer electronics to medical devices. Such aspects are of great importance, especially when it comes to bioelectronics, where compact and low-power circuits are essential for stable and reliable device operations[322–325].

Figure 4(b) illustrates high-density recording electrodes designed for stable neural signal acquisition[326]. Silicon neural probes, which leverage the precision and scalability of CMOS technology, are especially significant due to their ability to facilitate high-resolution, stable recordings essential for both research and clinical applications[287, 327]. CMOS technology enables these probes to achieve low power consumption and miniaturization, which are critical for long-term neural interfacing and device implantation[328]. Moreover, CMOS technology plays a pivotal role in the advancement of flexible electronics, particularly through its integration with innovative flexible manufacturing processes such as transfer printing and the use of flexible substrates like polyimide (PI). As shown in **Figure 4(c)**, analog circuits designed for electrophysiological signal processing can be fabricated using such techniques[111]. Following the doping process in conventional on-wafer manufacturing, the CMOS circuits can be transferred onto flexible substrates through precise transfer processes, which maintain the integrity of the circuits while allowing them to bend and flex. This approach enables the creation of high-performance, active-array flexible electrocorticography (ECoG) devices, which are capable of capturing detailed brain activity patterns with great precision and flexibility. These advanced ECoG arrays offer significant advantages over traditional rigid devices by providing better conformability to the brain's surface, reducing the risk of damage to neural tissue, and improving the quality of recorded signals. Such innovations hold significant potential for applications in brain-computer interfaces (BCIs), neuroprosthetics, and advanced neurological diagnostics[329–330].

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The piezoresistive effect in crystalline silicon is significantly influenced by the doping concentration[331–332]. The concentration of dopants within the silicon lattice determines the density of charge carriers-either electrons in n-type or holes in p-type silicon-which directly impacts the material's electrical response to mechanical strain (**Figure 4(d)**). At lower doping concentrations, the piezoresistive effect is more pronounced because the higher mobility of charge carriers allows for a greater change in resistance under strain[333–334]. This increased sensitivity occurs because fewer scattering events impede the movement of charge carriers, resulting in a more substantial alteration in conductivity when strain is applied[43, 335]. As a result, silicon with lower doping concentrations exhibits higher gauge factors, making it more responsive to mechanical deformations. Conversely, at higher doping concentrations, the increased number of charge carriers leads to more frequent scattering within the lattice[336]. This scattering reduces carrier mobility, thereby dampening the piezoresistive effect[337]. The result is a lower gauge factor, where the change in resistance in response to strain is less significant[338]. Thus, the sensitivity of the piezoresistive effect decreases as doping concentration increases. The gauge factor of silicon-based strain gauges, particularly when doped and fine-tuned, is significantly higher than that of conventional materials like metals[339].

The influence of doping concentration is further compounded by the crystallographic orientation of the silicon. Silicon, as a crystalline material, has specific atomic arrangements depending on its orientation, such as [100], [110], and [111] directions[340]. Each orientation exhibits different mechanical and electronic properties under strain, leading to variations in the piezoresistive response[341–343]. For instance, in the [110] orientation, silicon typically exhibits a higher gauge factor compared to the [100] orientation. This is due to the anisotropic nature of silicon's crystal lattice, where the deformation and corresponding changes in electronic properties vary based on the direction of the applied strain[344–346]. The total piezoresistive coefficient can be calculated using the sum of individual piezoresistive coefficients, each of which is weighted differently depending on the silicon orientation[347]:

$$\pi_{total} = \sum \pi_i \cdot W_i(\theta) \quad (1)$$

Where π_i represents the piezoresistive coefficient for each crystallographic direction, and $W_i(\theta)$ are the orientation-dependent weighting factors that describe how much each coefficient contributes based on the silicon crystal orientation, as depicted in **Figure 4(e)**. This orientation dependency, combined with the chosen doping concentration, enables the fine-tuning of silicon's piezoresistive effect for specific applications.

Building on the concept of orientation dependency in crystalline silicon, Won *et al.* demonstrated a highly accurate and multi-axis configurable strain sensor[348]. This work utilized the orientation-dependent piezoresistive properties of silicon nanomembranes (SiNMs) and a multiple transfer process technique to enhance the sensor's performance (**Figure 4(f)**). In their approach, Won *et al.* transferred SiNMs with two different crystallographic orientations, [100] and [110], onto a single flexible substrate. The [110] oriented silicon was chosen for its high piezoresistive sensitivity—approximately ten times greater than that of [100] oriented silicon—making it particularly effective for applications requiring precise strain detection[349]. By aligning these SiNMs along the same longitudinal direction of strain within a Wheatstone bridge circuit, they were able to exploit the distinct mechanical properties of each orientation to improve the overall sensor accuracy. **Figure 4(g)** shows experimental strain response testing where the [110] oriented SiNM displayed significantly higher sensitivity under longitudinal strain, confirming its role as the primary sensing element. Conversely, the [100] oriented SiNM showed much lower sensitivity under the same conditions. Additionally, the [110] oriented SiNM exhibited a negative piezoresistive response under transverse strain, a behavior consistent with the expected anisotropic nature of silicon's crystal lattice. The strategic use of these two orientations within the Wheatstone bridge configuration allowed for the development of a sensor capable of multi-axis strain detection, offering a new level of precision in strain sensing technology by combining the high sensitivity of [110] silicon with the more stable but less sensitive [100] orientation.

Along with the piezoresistive effect, temperature plays a significant role in the electrical conductivity of crystalline silicon[350–351], with the temperature coefficient of resistance (TCR) being crucial, particularly within the room to moderate temperature range important for flexible bioelectronics (**Figure 4(h)**)[352–354]. The TCR of silicon can be significantly enhanced through doping, enabling doped silicon sensors to exhibit higher sensitivity and precision in temperature measurement compared to conventional metal-based sensors, owing to the tunability of their electronic properties and reduced thermal noise in the crystalline lattice. In lightly doped silicon, TCR is generally positive, meaning resistance increases with temperature due to the relatively high mobility of charge carriers and increased scattering effects[355–356]. However, as doping concentration increases, TCR can become neutral or slightly negative[357]. In this case, the high density of charge carriers leads to more significant scattering from phonons and ionized impurities, reducing carrier mobility and stabilizing or slightly decreasing resistance as temperature rises[358].

Leveraging this temperature dependency of crystalline silicon, significant research has been conducted on flexible, high-accuracy temperature sensors based on crystalline silicon p-n diodes[359]. By optimizing doping levels and refining the transfer process, researchers have developed a highly sensitive flexible temperature array (**Figure 4(i)**)[115]. This array demonstrates excellent thermal mapping capabilities, closely matching the temperature distribution generated by an underlying copper heater. The silicon diode temperature sensor provides high sensitivity and stability, making it highly effective for precise temperature monitoring in flexible electronic applications[360]. **Figure 4(j)** shows temperature dependency of the fabricated flexible crystalline silicon p-n diode. As the temperature increases, the currents through the diode increase, which can be expressed by the Shockley equation:

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$$I = I_s(e^{\frac{qV}{kT}} - 1) \quad (2)$$

Here, I_s represents the reverse saturation current, which increases exponentially with temperature as:

$$I_s \approx T^3 e^{-\frac{E_q}{kT}} \quad (3)$$

As the doping concentration increases, the temperature dependency of carrier mobility decreases. Even though the mobility of silicon decreases with increasing temperature, the increase in saturation current overshadows this effect, resulting in an overall increase in the current flow through the diode[361].

Since crystalline SiNM responds to both applied strain and temperature changes, it can be integrated into a multifunctional sensor system[362]. A bioresorbable intracranial sensor was developed to monitor both temperature and pressure (**Figure 4(k)**)[118]. They utilized a single SiNM via a single transfer process, aligning the pressure-sensing parts of the SiNM onto a prepared cavity structure. This cavity structure allowed the measurement of applied pressure by deforming the floating SiNM under pressure, effectively creating a strain response. This work highlights how stable and highly sensitive single-crystalline silicon can be optimized and functionalized through advanced fabrication methods, paving the way for multifunctional sensor systems in bioelectronics[363].

Doping in crystalline silicon not only influences its electrical and thermal properties but also modulates its optical characteristics[364–365]. Changes in the refractive index due to increased free carrier concentration affect light propagation and absorption. Additionally, photoluminescent properties can be tailored through dopant type and concentration, enhancing radiative recombination in specific wavelength ranges. Lastly, the plasmonic behavior of doped silicon enables improved light trapping capabilities, a key advantage for solar cell applications.

2.3 Perspective

2.3.1 Perspective for oxidation

Pre-oxidation cleaning:

It is critical to avoid contaminants throughout the entire micro/nano fabrication process of silicon electronics, to ensure the reliability and performance of the products[366–368]. For high-temperature procedures such as thermal oxidation of silicon, unwanted contaminants can not only ruin individual samples but also adversely affect other samples within the batch[369–371], or even the entire equipment, by inflicting irreversible damage to the processing chamber[372–374]. Due to the mechanism of thermal oxidation, which consumes a proportion of the silicon wafer to directly form an oxide layer on the silicon surface[375–376], even minor particles or contaminants pre-existing on the surface can result in defects among the oxide layer or the Si/SiO_2 interface[377]. These defects eventually develop in the form of initiation points for physical cracks or fractures during subsequent processes[378–379]. They also lead to functional failures of the t-SiO_2 layer, such as the penetration of contaminants when used as a barrier, and the occurrence of oxide charges (e.g., oxide trapped charge, fixed oxide charge, and interface trapped charge) when used as a gate dielectric of a MOSFET[380–383]. Therefore, pre-oxidation cleaning is critical to obtain a clean silicon surface for the thermal oxidation, as this plays a significant role in determining the quality of the t-SiO_2[285, 384–385].

A commonly employed pre-oxidation cleaning strategy involves chemically cleansing the silicon surface[284]. This includes applying the standard Radio Corporation of America (RCA) cleaning process, where a mixture of ammonium hydroxide and hydrogen peroxide is used to remove organic matter, followed by hydrochloric acid and hydrogen peroxide to eliminate metallic ions[386–389]. Another approach is utilizing piranha solution, a mixture of sulfuric acid and hydrogen peroxide, with a subsequent immersion in hydrofluoric acid to remove the thin native oxide formed on the surface[390–391]. The final hydrofluoric acid treatment immediately prior to oxidation is an essential step, as it removes the native oxide layer present on the silicon surface and imparts hydrophobicity to the hydroxylated wafer[392], which would otherwise be hydrophilic and unsuitable for the formation of a high-quality Si/SiO_2 interface[393].

Other strategies for pre-oxidation cleaning include growing and subsequently removing a sacrificial oxide layer before the main process[394–395], dry cleaning with ultraviolet (UV)/ozone treatment[396–397], or employing megasonic cleaning with ultrasonic generators[398]. One or more of these approaches are often combined to enhance the immaculateness of the surface, with careful attention to the sequence of the processes, ensuring that the final step does not leave any residual layers on the silicon surface.

Oxidation parameters:

The thickness of the t-SiO_2 layer grown on the silicon surface is determined by various factors. Manufacturers performing thermal oxidation using a tube furnace must undergo a relatively manual operation of extracting the sample from the tube, after a predetermined period of time at a preset temperature[399]. During this process, a considerable extent of temperature fluctuation within the processing chamber is virtually inevitable, since the sample holder (or 'boat') is exposed to the ambient environment during the loading/unloading procedure[400–402]. Therefore, in order to grow an oxide layer with optimal thickness suitable for its intended use, it is important to be familiar with the different parameters that affect the thickness of t-SiO_2.

Key factors that influence the thickness of the oxide layer include the temperature, pressure, and oxidation time within the tube furnace where thermal oxidation occurs[403–404]. The effects of these factors on the determination of oxide layer thickness have been well-documented and summarized in numerous references[405]. Additionally, other parameters that should be considered during the oxidation process due to their impact on the oxide thickness include: orientation of the silicon wafer[406], doping profile of the wafer[407–408], and atmosphere (wet/dry) of the oxidation process[194]. The growth rate of t-SiO_2 varies depending on the orientation of the silicon wafer, as the number

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of silicon bonds per unit area differs with crystal orientation[409]. The numbers of Si bonds per cm^2 in the orientation of [100], [110], [111] are 6.8 × 10^{14}, 9.6 × 10^{14}, and 11.8 × 10^{14}, respectively[410]. Doping also influences the oxidation rate, with both p-type and n-type doping generally accelerating the formation of t-SiO_2[411]. This trend is due to the increased diffusion rate of oxidants in the case of n-type doping and the increased vacancy inside the silicon in the case of p-type doping[412–413]. It is well known that wet oxidation, with H_2O in the form of steam, results in a faster growth rate of the oxide layer, whereas dry oxidation, which relies solely on high-temperature oxygen gas, produces a slower but higher-quality oxide layer[414].

It is also worth noting that the growth rate of t-SiO_2 with a very thin thickness of just a few hundred angstroms does not follow the trends predicted by the aforementioned DG model[415]. The oxidation rate during the initial oxidation stage is more than twice as fast as Deal and Grove predicted, due to the different kinetic models applied to the oxidant diffusion across the oxide layer[416–417]. Therefore, in cases where a very thin t-SiO_2 layer is required, such as for a gate dielectric of a MOSFET in modern microelectronics, the process parameters should be determined based on the Massoud model, rather than the DG model[418].

2.3.2 Perspective for doping

Diffusion doping of thin silicon for flexible electronics

Diffusion is a well-established doping method that remains fundamental in semiconductor manufacturing due to its reliability in modifying silicon's electrical properties. Unlike ion implantation, which precisely injects dopants, diffusion introduces dopants at the silicon surface, driven by thermal energy, progressing inward based on temperature and time[264–265, 419].

While diffusion doping is critical, it presents unique challenges, especially in flexible electronics. Proper control of diffusion is essential to ensure uniform doping profiles, which directly impact device performance[420]. The drive-in process is crucial for achieving uniform profiles, but it must be carefully managed, particularly in thin silicon membranes, to avoid unwanted effects[421].

A well-controlled diffusion process also enables vertical double-sided doping, which is valuable in applications requiring precise junctions, such as PIN structures in photovoltaic devices[144]. However, achieving such precision in thin silicon membranes is challenging due to difficulties in controlling the depth and distribution of dopants on both sides. Careful management of temperature and time during diffusion is essential to overcome these challenges and create high-performance flexible silicon-based devices[408, 422].

In scenarios requiring patterned doping, such as in the fabrication of diodes, transistors, and MOSFETs, substrate transfer processes present specific challenges. High-temperature diffusion often leads to thermal oxidation, forming a thick oxide layer on exposed silicon areas. Removing this oxide layer post-doping can create a surface step between doped and undoped regions due to differential oxidation. This step can introduce mechanical fragility during substrate transfer, particularly in flexible electronics, where even slight surface irregularities can compromise device integrity. Optimizing doping and oxidation conditions is crucial to minimize these risks and ensure the reliable performance of flexible silicon-based devices.

Metal dopants

Doping materials and their roles in the silicon atomic structure are fundamental to determining silicon's electrical, mechanical, and optical properties[295, 299, 306, 317]. In classical doping, elements like phosphorus (for n-type) and boron (for p-type) are integrated into silicon to modify its electrical characteristics by creating regions rich in electrons or holes[250]. These dopants are chosen for their compatibility with the silicon lattice and their predictable effects on electronic behaviour. However, as applications evolve, particularly in bioelectronics, where devices need to be flexible, wearable, and biocompatible, traditional dopants often fall short of meeting these stringent requirements.

In these advanced contexts, non-classical doping methods, such as doping with metal ions like gold (Au), become necessary[423]. Metal ion doping introduces deep-level traps within the silicon bandgap, significantly influencing carrier lifetimes and recombination processes[424]. For instance, Au doping in p-type silicon introduces deep acceptor levels that trap electrons, effectively reducing free hole concentration and increasing recombination rates. This altered electronic behaviour can enhance sensitivity to temperature variations, making Au-doped silicon particularly useful in high-precision temperature sensors critical for bioelectronic applications. Furthermore, Au doping improves device performance in high-radiation environments by stabilizing carrier lifetimes, making it a strong candidate for radiation-hardened electronics. By carefully modulating the concentration and distribution of gold within silicon, one can tailor these properties to suit various applications, including high-temperature sensors, radiation-hardened electronics, and fast-switching components in advanced electronic devices.

Other metal dopants, such as iron (Fe), copper (Cu), magnesium (Mg), and nickel (Ni), also play unique roles in silicon doping[424–426]. Each introduces distinct deep-level states, offering opportunities to fine-tune silicon's properties for specific uses. For instance, Fe doping can create trap states that improve charge storage capabilities, while Cu doping might be leveraged for its impact on silicon's thermal properties. Understanding and exploiting these unconventional doping methods are key to advancing silicon's functionality in next-generation bioelectronic devices.

3. Rigid to Soft

The transformation of rigid crystalline silicon into flexible functional substrates represents a pivotal advancement in bioelectronics, enabling the seamless integration of electronic devices with the soft and flexible nature of biological tissues[114].

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This transition is primarily achieved through two key methods: the substrate transfer process and the device transfer process (back-side silicon etching). These processes are crucial for adapting crystalline silicon—a material traditionally known for its rigidity—into flexible, biocompatible forms without compromising its exceptional properties[139]. This section will introduce these approaches, highlighting both conventional and unconventional methods, materials, and applications, while also discussing the critical technical points and considerations necessary for their practical implementation in advanced bioelectronic devices.

3.1 Substrate transfer process

The substrate transfer process is critical for transforming rigid crystalline silicon into flexible substrates, enabling its use in advanced bioelectronics[134]. This process involves a sequence of precise detachment and reassembly of active silicon layers onto biocompatible, flexible substrates, which allows silicon to maintain its high electronic performance while gaining the necessary flexibility for wearable and implantable applications[427–434].

The flexibility of SiNMs is achieved by reducing the silicon layer's thickness, significantly decreasing its bending stiffness. This reduced stiffness is essential for applications where silicon must bend and conform to various shapes without breaking. The critical bending radius, which determines the extent to which the silicon can be bent without fracturing, decreases as the silicon becomes thinner, enabling its use in more complex and compact designs[93, 435–438].

The substrate transfer process for SiNMs onto flexible substrates includes several integrated steps[135]. First, the silicon layer is prepared on SOI or bulk wafers, where it is thinned and patterned using processes such as oxidation and etching. Next, the silicon layer is released from the wafer by etching away the underlying sacrificial layer, isolating the active membrane. This membrane is then transferred onto a flexible substrate using a stamping process. Finally, post-transfer processing, including patterning and metallization, is conducted to complete the fabrication of the electronic device. This seamless integration ensures that silicon maintains its high electronic performance while acquiring the flexibility necessary for bioelectronic applications.

In this section, we explore the specific advantages of integrating silicon into flexible bioelectronics, detailing how these benefits align with each step of the substrate transfer process. We will discuss how the preservation of silicon's inherent properties is maintained during the preparation of the silicon layer, how mechanical flexibility is enhanced as the silicon is thinned down during the release from the wafer, and how the critical transfer process ensures the active silicon layer is adapted to various flexible substrates without compromising functionality, ultimately leading to high-performance bioelectronic devices. This process is essential for creating flexible electronics that retain silicon's high performance while enabling adaptability for applications requiring flexibility and durability. It also enables the development of devices that can conform to complex surfaces, such as the human body, making it particularly valuable in bioelectronics. Furthermore, the substrate transfer process allows to produce large-area, flexible silicon devices, paving the way for advancements in wearable and implantable healthcare technologies[428].

3.1.1 SOI vs bulk

The substrate transfer process begins with the decision of whether to use SOI wafers or bulk silicon wafers, as each differs significantly in the manufacturing process and presents distinct advantages, which directly relate to the final application of the device (**Figure 5(a)**). SOI wafers are typically preferred for applications with stringent performance requirements, due to the inherent advantages offered by their structural characteristics[439–441]. SOI wafers consist of a thin silicon layer separated from the bulk silicon by a buried oxide (BOX) layer of SiO_2. This BOX layer acts as a sacrificial layer that can be selectively etched away using HF, allowing for the release of the SiNMs. Such ability to easily release ultrathin membranes with a tight control over their thickness is highly beneficial for applications that require high uniformity and minimal parasitic effects. Despite its thinness, the silicon membrane excised from the handling layer retains remarkable electrical properties, making it ideal for applications that demand both morphological flexibility and superior performance of the fabricated device. However, SOI wafers are generally more expensive than bulk silicon wafers, which can be a limiting factor for cost-sensitive applications or mass production[442].

As one of the two approaches, using bulk silicon wafers is generally more cost-effective but may entail further complex processing steps to achieve comparable results[73, 158, 244, 252]. Unlike SOI wafers, bulk silicon does not have a pre-existing sacrificial oxide layer, which necessitates additional processing steps such as ion implantation or chemical exfoliation to create a releasable silicon layer. Such interventions may increase the complexity and determinants within the process, potentially resulting in process-induced variabilities of the final product. However, the complexity of processing bulk silicon can lead to challenges in controlling the thickness and uniformity of the released silicon layer. Additionally, the lack of a built-in sacrificial layer means that the release process may introduce more defects, which can affect the performance of the final device. Nevertheless, distinct advantages of bulk wafers remain, particularly in terms of cost efficiency and the compatibility of CMOS processing techniques. Bulk silicon wafers are typically less expensive than SOI wafers, making them suitable for quantity production or cost-sensitive applications. Also, the well-controlled processing techniques used to release the silicon layer from bulk can produce a wide range of film thicknesses, facilitating adaptation to various biomedical applications. To address the drawbacks and balance between such trade-offs, future research should focus on developing advanced techniques that enhance process controllability, minimize layer defects, and ensure greater consistency in the quality of the transferred silicon layers.

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As an alternative strategy, the SOI wafer-based transfer process holds distinct advantages, making it particularly well-suited for applications that demand high precision and performance. The constitution of a pre-existing BOX layer not only provides manufacturing-related benefits but also opens possibilities for the usage of itself as a functional oxide layer. Such advantages when coupled with the ability to precisely control the thickness of uniform layers of silicon, render SOI wafers ideal for high frequency bioelectronic devices, where the minimization of parasitic capacitances is of critical importance. The inherent electronic properties of silicon, such as high carrier mobility, are preserved in this process, contributing to the development of highly efficient devices. In **Figure 5(b)**, Menard *et al.* introduced a method for creating high-performance, flexible thin-film transistors on plastic substrates using micro- and nanoscale single-crystal silicon devices from SOI wafers[134]. They patterned silicon into bars and ribbons on the SOI layer and removed the underlying SiO_2 through wet etching, then transferred the patterned silicon onto plastic substrates using a PDMS stamp. To prevent the released top silicon membrane (ink) from drifting during its release from the bulk silicon (donor), physical anchoring or van der Waals interactions between the ink and donor must be considered[140]. This crystalline silicon transfer to plastic process opened up new avenues for researchers to develop flexible electronic devices and apply them in various fields, thereby paving the way for new research areas. The concept of nano-meshed SiNMs, offering high-performance stretchable electronics, is depicted in **Figure 5(c)**[443]. They formed the top silicon of SOI into a mesh shape, applied a PI film layer, and used a PDMS stamp to transfer it onto a stretchable substrate. By converting silicon films into nano-meshes, they achieved high electron mobility and moderate stretchability. Despite the higher cost of SOI wafers and limitations in thickness variation, the advantages of precision and performance make SOI-based transfer method a key enabler in advancing flexible bioelectronics. Furthermore, silicon nanowires (SiNWs) fabricated using top-down lithographic methods, offer precise control over dimensions and alignment[444–447]. Once formed, these SiNWs can then be transferred onto flexible substrates, enabling high-sensitivity applications such as neural interfacing and biochemical sensing[448–450]. CMOS-compatible fabrication ensures scalability, making SiNWs a valuable addition to flexible bioelectronic platforms. Future research could focus on reducing costs and expanding the versatility of the process, potentially broadening its application in various bioelectronic technologies.

The bulk wafer approach is pursued primarily due to cost considerations and the potential for producing large quantities of SiNMs. The goal is to develop a more cost-effective method for creating flexible silicon layers without relying on the consumption of expensive SOI wafers. A simple and effective process for mass-producing high-quality single-crystal silicon micro- and nanoribbons from bulk silicon [111] wafers is highlighted in **Figure 5(d)**[73]. The process involved first creating etched trenches with controlled ripple structures on the sidewalls. This was followed by angled evaporation of masking materials and anisotropic wet etching, such as KOH etching, achieving the desired thickness and uniformity. After these steps, the SiNRs were then transferred to various substrates. These SiNRs exhibited excellent electrical properties and significantly contributed to the advancement of transistors, sensors, and various flexible electronic applications based on bulk silicon. A cost-effective method was developed to produce ultrathin crystalline silicon membranes from a single wafer, allowing multiple transfers until the wafer is fully utilized (**Figure 5(e)**)[144]. These membranes, ranging from 300 nm to 13 μm in thickness, were successfully applied to flexible solar cells and n-channel metal-oxide-semiconductor (NMOS) transistor arrays, demonstrating potential for flexible electronics.

As shown, this bulk-based method is more cost-effective and scalable than the SOI-based approach, making it suitable for lab-to-fab applications or large-scale productions. However, the absence of a built-in sacrificial layer may increase the vulnerability against defects throughout the prolonged manufacturing process, which can affect the performance of the final device[451]. To overcome these challenges, future research must head towards developing advanced processing techniques that can improve the nanoscale controllability over uniformly produced silicon films and reduce the likelihood of unwanted defects. The discussed examples illustrate how the substrate transfer process has enabled the transformation of rigid silicon into flexible forms, significantly advancing the field of flexible electronics. The technological innovations highlighted in each case underscore the broad applicability of the sophisticated process in bioelectronics.

Both the bulk-based and SOI-based approaches accompany distinct advantages and limitations among the transfer process. From the perspective of production, the decision between the two methods should be made based on the requirements of the final device and its application. Various factors and constraints such as production price, performance, and precision may influence the decision of manufacturers.

3.1.2 Pick-up process

The pick-up process, as illustrated in **Figure 6(a),** is a critical step in fabricating flexible devices, involving the delicate detachment of a thin crystalline silicon layer from its original wafer. This process can be achieved through methods such as selective etching, ion slicing, or laser lift-off, all aiming to ensure the uniformity and defect-free nature of the released silicon layer. The key tool in this process is typically a polymer-based elastomer stamp (e.g., a PDMS stamp), which must maintain strong adhesion while allowing for clean separation without damaging the silicon membrane[136, 139, 430, 452–453].To successfully detach the thin silicon film, typically but not always patterned, it is essential to optimize several manufacturing factors and parameters[139, 428]. To begin with, ensuring the uniformity of the on-wafer patterning process guarantees that the sacrificial layer is etched evenly, allowing for the top silicon layer to be consistently released. Proper alignment of the stamp with the patterned silicon is also a crucial consideration, in order to prevent any misalignment or stress concentration that could lead to defects or fractures during the peel-off procedure.

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Additionally, controlling the peeling rate and angle is important to minimize mechanical stress applied on the silicon layer, further reducing the risk of unwanted damage. By carefully considering these factors, a high-quality transfer of the silicon layer, which is a critical prerequisite for the performance and reliability of flexible electronic devices, can be achieved[454].

Furthermore, optimizing the release process requires careful management of the interfaces between the stamp and silicon layer, as well as between the top and bottom silicon layers after the sacrificial layer is removed[244, 455]. Ensuring appropriate adhesive strength at such interfaces, controlling surface energy, and maintaining cleanliness are vital for reducing unwanted defects or delamination. Matching the mechanical properties of the materials involved throughout the procedure is crucial for inducing minimal stress, which in turn prevents damage while picking up the silicon layer[456–458]. Properly managing these factors across different layers ensures that the silicon membrane is released smoothly, preserving the integrity of the thin film and resulting in a successful, defect-free transfer[73, 108, 136, 430, 459–464].

The mechanics of this process are deeply rooted in the understanding of kinetically controlled transfer printing, as explored by Feng *et al.*, who focused on the competing fracture between the ink/stamp and ink/substrate interfaces (**Figure 6(b)**)[460]. They developed a theoretical model based on the energy release rate that predicts the critical peel velocity (V_c), which determines whether the ink is picked up from the donor substrate or printed onto the receiving substrate. If the peel velocity is above V_c, the film is picked up by the stamp; if below, the film remains on the substrate. The adhesion between the stamp and the film is strongly dependent on the rate at which the stamp is peeled away. The viscoelastic nature of the PDMS stamp means that its adhesion strength increases with peeling velocity, a relationship that is modelled mathematically. The study also emphasized the crucial role of peel velocity and temperature in optimizing the transfer process. They have found that lower temperatures are optimal for picking up objects, while higher temperatures facilitate printing, ensuring reliable and precise control in the scalable transfer of thin films and microdevices. At temperatures above the glass transition temperature (T_g) of PDMS, the material becomes more flexible and compliant due to reduced stiffness[465]. This increased compliance enhances conformal contact between the PDMS stamp and the target substrate, improving adhesion and facilitating the transfer printing process. The reduced stiffness also minimizes energy loss during detachment, ensuring smooth and reliable adhesion and release. The theoretical framework established by this study provides a critical foundation for optimizing crystalline silicon-based transfer processes. Furthermore, elevated temperatures can facilitate the transfer process by decreasing the adhesion between the PDMS stamp and the Si membrane[466]. In addition to the crucial role played by the stamp in the pick-up process, a thorough understanding of the interfaces between the layers is also essential. A pattern transfer method for thin silicon membranes, using self-delamination driven by interfacial design in liquid media, acetone, is shown in **Figure 6(c)**[467]. A controlled peeling process in liquid media, where the thin film's detachment is driven by interfacial forces. The process can be tuned by adjusting surface energy, wettability, and porosity. This technique allows the precise transfer of pre-patterned device-grade silicon onto various substrates, facilitating integration into multi-functional systems. The method enables multiple lithography steps on both sides of the silicon membrane, which can be flipped and reprocessed as needed. The process is particularly effective for applications requiring both front and back-side integration, such as microelectromechanical systems and metamaterials, highlighting the flexibility of the approach. In addition to the commonly used PDMS stamps, unconventional stamps with specialized properties are also employed to enhance the versatility and precision of the transfer printing process.

As depicted in **Figure 6(d)**, a programmable and scalable transfer printing technique was developed, utilizing a shape-conformal stamp with thermally expandable microspheres embedded in an adhesive layer[137]. The shape-conformal stamp, consisting of a bilayer thin sheet with a polymeric backing and an adhesive matrix containing expandable microspheres, utilizes an automated laser heating system to selectively control its adhesion. The laser system triggers the expansion of the microspheres, reducing adhesion where needed, allowing for accurate and programmable placement of delicate electronic elements onto flexible surfaces. This method enables programmable, large-area integration of ultrathin, delicate components with high yield and reliability. The approach is particularly suited for manufacturing flexible electronics and offers significant scalability, though improvements in adhesion control and resolution are needed for even finer components. Additionally, the technique may cause thermal degradation in temperature-sensitive devices; hence, further optimization is needed. An innovative transfer printing technique using shape memory polymer (SMP) stamps for flexible and stretchable electronics is presented in **Figure 6(e)**[468]. This technique uses a low-power laser to trigger shape memory effects in SMPs, enabling precise, spatio-selective transfer of electronic microelements onto soft substrates with perfect yields. It is highly scalable, suitable for large-scale manufacturing due to its programmable nature and independence from retraction speed. Additionally, it excels in hybrid printing, allowing simultaneous transfer of different materials like silicon and GaAs, effectively overcoming challenges associated with interfacial adhesion differences. This temperature-controlled process, unlike traditional velocity-based methods, offers exceptional control and scalability, making it ideal for producing sophisticated flexible electronics, including hybrid devices with diverse materials. It represents a significant advancement in manufacturing, combining precision with the ability to achieve large-scale production with perfect yield and minimal component damage. The pick-up process is far more than just a simple mechanical operation, but a critical and highly optimized step, grounded in a deep understanding of material science and process engineering, essential for the successful fabrication of advanced flexible bioelectronic devices.

3.1.3 Transfer printing process

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As visualized in **Figure 7(a)**, the transfer process is a critical step of integrating thin silicon layers onto flexible substrates, such as polymers or biodegradable materials, to maintain its characteristics as an excellent electronic component, while granting it the ability to conform to surfaces with complex geometries. In this process, precise control over adhesion is paramount to ensure that the silicon adheres firmly to the substrate without its structure being damaged. Beyond simply being extra cautious, practical methods, such as incorporating buffer layers and considering mechanical factors-such as adjusting the speed and angle of transfer-are employed to enhance adhesion and prevent damage. These approaches guarantee that the silicon layer maintains its integrity and preserves its original material properties throughout the process[77, 136, 202, 430, 460–461, 463, 468–471].

Selecting the appropriate substrate is also a vital factor for such meticulous transfer printing and the successful utilization of the fabricated device. The requirements of the substrate, determined by the operating environment of the device-whether it should be stretchable[360, 472], transparent[138, 443, 469, 473–475], or bioresorbable[110, 362, 476–481]-dictate suitable materials that can be used as the substrate layer in the printing process. Depending on the characteristics of the substrate, adjustments to the transfer technique may be necessary to optimize the adhesion and functionality of the silicon layer. By carefully tailoring both the substrate and the transfer method, rigid, fragile single-crystal silicon can be transformed into a flexible, durable component suitable for advanced biomedical and wearable devices.

In this section, we examine how recent studies have optimized the transfer process to preserve the structural and functional integrity of silicon layers. Specifically, we will focus on the critical interface between the stamp and substrate, highlighting the role of techniques to modify the adhesion, such as adopting buffer layers or making mechanical adjustments to enhance the precision of the transfer. Additionally, we will explore how the selection of substrates, tailored to specific device applications, influences both the transfer process and the overall performance of the final device.

As shown in **Figure 7(b)**, a stretchable electronic circuit design, using single-crystalline silicon in a non-coplanar mesh layout, enables stretching up to 140% while maintaining electrical performance[482]. The key to this success was the precise control over the transfer process, particularly the use of Cr/SiO_2 as an adhesion layer that ensured the silicon nanomaterials adhered securely to the polymer substrate. This layer not only facilitated the transfer but also protected the circuits from damage during mechanical deformation. Furthermore, an additional adhesion treatment can be applied to the receiving substrate before transfer to enhance bonding. For example, a PI layer[257] or ozone treatment[483] has been shown to create surface conditions conducive to strong adhesion. The integration of these methods provides robust mechanical stability and enables high-performance flexible and stretchable electronic systems. The stretchable electronic study's transfer process involved doping and patterning SiNRs on SOI wafers, followed by their transfer onto a pre-strained PDMS substrate. The use of serpentine bridge interconnects to connect circuit islands further enhanced the stretchability and durability of the circuits, allowing them to conform to complex, curved surfaces. This approach has significant implications for the development of wearable and implantable devices, where flexibility and durability are crucial. **Figure 7(c)** introduces a novel adhesive-less transfer printing technique, which uses the controlled bending radius of a flat elastomeric stamp to transfer microscale semiconductor materials onto various substrates[484]. This method eliminates the need for interlayer adhesives, which are often used in traditional transfer printing methods but can limit processing temperatures and introduce electrical or thermal resistance. The bending radius of the PDMS stamp is adjusted to either pick up or print micro sized Si plates onto the target substrate. A smaller bending radius increases the applied pressure while reducing adhesion, promoting the successful transfer of the micro Si plates onto the target substrate. Conversely, a larger bending radius decreases pressure and enhances adhesion, making it more suitable for picking up micro Si plates from the donor substrate. This mechanical control allows for precise placement of the silicon plates, ensuring high-quality integration onto surfaces as diverse as rigid glass, flexible films, and curvilinear objects like eyeglasses and bluetooth earphones. This technology is particularly advantageous for applications requiring high-temperature processing or processes that cannot use intermediate layers, as it allows for the transfer of semiconductor materials of various sizes and shapes without alignment errors or damage. The absence of adhesives reduces the potential for contamination and defects, resulting in cleaner and more reliable electronic interfaces. This method represents a significant advancement in the field of flexible and stretchable electronics, offering a simpler and more effective approach to the transfer of high-performance electronic devices.

The use of bioresorbable silicon pn diodes for optoelectronic neural modulation, focusing on the precision required in the transfer process to ensure the functionality of these delicate devices, is explored in **Figure 7(d)**[479]. The study involved fabricating thin-film monocrystalline silicon diodes capable of generating polarity-dependent photovoltages under laser illumination. These photovoltages could either excite or inhibit neural activities, offering a non-invasive means of neuromodulation. The transfer process was critical in this context, as the diodes needed to be carefully placed onto neural tissues without compromising their performance or the biocompatibility of the final device. The researchers used PDMS stamps to transfer the silicon diodes onto flexible, biocompatible substrates, polyethylene terephthalate (PET) films, which were then implanted onto neural tissues. The thin and transparent nature of the substrates facilitated secure implantation and ensured seamless integration with tissues and organs, enabling a wide range of applications in biological sensing and neural modulation. The study demonstrated that precise control over the transfer process, including the use of mechanical adjustments and careful substrate selection, was essential in achieving reliable optoelectronic modulation of neural activity. This work opened new possibilities for the development of advanced

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biomedical devices that can interact with the nervous system in a controlled and minimally invasive manner. Yu *et al.* demonstrated the use of bioresorbable silicon electronic arrays for transient spatiotemporal mapping of electrical activity in the cerebral cortex (**Figure 7(e)**)[485]. The focus of their research was on creating electrode arrays that could be implanted on the brain's surface to record electrophysiological signals while gradually dissolving over time, thereby eliminating the need for surgical extraction. The transfer process was a crucial aspect of this work, as it involved moving thin, flexible SiNMs onto a biodegradable polymer substrate, specifically polylactic-co-glycolic acid (PLGA), which would then conform to the brain's surface. The use of PI as an adhesion layer during the transfer ensured that the SiNMs adhered securely to the substrate, while subsequent RIE dry etching removed the PI layer, leaving behind a fully bioresorbable device. The researchers carefully controlled the dissolution rates of the silicon and encapsulation materials to match the intended lifespan of the device, ensuring that it would remain functional during the critical period of neural monitoring before safely dissolving within the body. The study demonstrated that through meticulous optimization of the transfer process, it is possible to integrate sophisticated electronic systems into bioresorbable platforms, paving the way for new applications in transient neural interfaces and other temporary medical implants. These case studies collectively emphasize the importance of optimizing the transfer process in the development of advanced electronic devices. Whether for achieving extreme mechanical flexibility, eliminating the need for adhesives, or ensuring biocompatibility and biodegradability, the choice of adhesion techniques, substrate materials, and mechanical controls plays a critical role in the success of the final device. Through these detailed investigations, it becomes clear that transfer printing is not merely a process of technically relocating the silicon layer onto a foreign platform, but rather a fundamental aspect designed and realized to enable the implementation of cutting-edge electronic devices in various biomedical applications.

3.1.4 Flexible manufacturing

After the substrate transfer process of a crystalline Si membrane, the device undergoes further manufacturing steps to attain its final form, tailored to its specific applications. (**Figure 8(a)**) These processes generally fall into three fundamental stages: silicon isolation, metallization for interconnection, and device encapsulation[237].

The first stage, silicon isolation, involves defining the geometric shape of the silicon, which is typically achieved through conventional photolithography patterning. Since most substrate transferred silicon-based sensors are small, the mechanical and electrical properties of silicon can be significantly affected by its shape, making micro-scale fabrication techniques critical. However, many flexible substrates, often composed of polymers, are not compatible with strong acidic or alkaline solutions[486–488], which precludes the use of wet-etch processes for crystalline silicon. Consequently, dry etching using a RIE system becomes the preferred method for shaping the silicon[434, 451, 489–490]. Silicon isolation serves critical functions in flexible bioelectronics, particularly in logic circuits like diodes or transistors. It prevents electrical interference, such as crosstalk, by ensuring that each device operates independently, which is crucial for maintaining signal integrity. Additionally, isolation aids in thermal management by preventing heat from spreading to adjacent devices, thus preserving their performance. Finally, it enhances device reliability and longevity by minimizing the impact of electrical stress and leakage currents over time[115, 118, 162, 352, 485].

Along with these electrical isolation perspectives, the mechanical considerations of silicon-based flexible bioelectronics are equally important[85, 244, 491–492]. Flexible bioelectronics are often exposed to significant strain or deformation, and silicon, being a brittle inorganic material with a high Young's modulus, is susceptible to mechanical failure. To address this issue, the silicon membrane can be strategically patterned into shapes like serpentine structures or placed in regions of minimal strain, such as within island structures[493-495]. For example, as shown in **Figure 8(b)**, a serpentine SiNMs design is used for a stretchable strain sensor[339]. Kim *et al.* demonstrated that with a serpentine structure integrated onto a flexible PI substrate, the silicon experienced minimal stress even under 30 % applied strain, significantly reducing the risk of mechanical failure. This design strategy can be used for biaxial strain mapping (**Figure 8(c)**). **Figure 8(d)** provides the detailed illustration of the effectiveness of directional sensitivity in strain sensors, demonstrating how the specific orientation of the sensors dramatically influences their responsiveness to applied strain. The strain sensor oriented horizontally (indicated in blue) is significantly more responsive to strain applied in the horizontal direction, while showing minimal change when subjected to vertical strain. Conversely, sensors oriented vertically demonstrate greater sensitivity to vertical strain. This innovative structural design greatly enhances the ability of silicon to detect mechanical changes, allowing for more precise and reliable strain measurement in flexible bioelectronics[45, 115, 496–498].

On a flexible substrate, the isolated silicon must be connected either to external measurement instruments or to other silicon cells[93, 499]. However, even when silicon is highly doped with its conductivity greatly enhanced, it still exhibits poor interconnection performance compared to metals, resulting in high line impedance and low compatibility with normal interconnection methods such as wire bonding or soldering. Therefore, metallization of silicon is crucial for creating stable electrical contacts, which should ideally form Ohmic contacts[92, 114, 118, 146, 482, 500–504]. When forming heterojunctions between the semiconducting silicon membrane and conductive metal, the choice of metal depends on the doping type of the silicon (**Figure 8(e)**). For n-type silicon, metals with a lower work function than that of silicon are preferred to ensure making Ohmic contacts. Commonly used metals for n-type silicon include aluminium (Al), titanium (Ti), and chromium (Cr)[350, 500]. These metals effectively create Ohmic contacts by having a lower work function, allowing electrons to flow easily from the metal into the conduction band of n-type silicon. For p-type silicon, metals with a higher work function than that of silicon

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are considered to achieve Ohmic contacts[504]. Suitable metals compatible for p-type silicon include gold (Au), platinum (Pt), and nickel (Ni). These metals are chosen because their higher work functions reduce the energy barrier, facilitating efficient charge carrier (hole) movement across the metal-silicon junction.

Various methods are available for metallization on isolated silicon on flexible substrates, including physical vapor deposition (PVD) techniques such as sputtering or thermal evaporation, chemical vapor deposition (CVD), electroplating, and screen printing[237, 291, 293, 316, 362, 488, 505]. When choosing a method among multiple options, it is important to consider the compatibility with the substrate, ensuring that the processing temperature does not exceed the substrate's thermal allowance. A sequence of deposition and photolithographic patterning is commonly used due to its compatibility with various polymer substrates and its ability to achieve high spatial resolution. However, when it comes to the realm of bioresorbable electronics, where the narrowly selected substrate material may also be vulnerable to solution-based processing, alternative manufacturing strategies must be considered[506–508]. A specific approach using paste-based electrical contacts was used to achieve metallization with silicon and metal foils for bioresorbable electronics. (**Figure 8(f)**)[121]. They utilized a hot-press method to achieve chemical and electrical integration of each electronic component on a synthesized polyurethane-based bioresorbable substrate. The fabricated silicon diode was successfully connected to the power coil and stretchable electrodes for electrical stimulation.

This method relies on the unique properties of the conductive paste, which plays a crucial role in ensuring both electrical connectivity and biocompatibility. The paste typically comprises conductive particles, such as silver or carbon, dispersed in a polymer matrix. This combination balances electrical conductivity with biocompatibility, making it well-suited for bioresorbable electronics. When utilizing the conductive paste as an electrical contact between silicon and metal, several factors should be carefully considered[509]. First, its adhesion stability under harsh conditions such as humid and dynamic environments must be addressed. Additionally, as the paste is primarily applied manually, there is an inherent risk of human error, which may lead to inconsistencies in the application compared to automated metal deposition methods.

The requirement that all components, including silicon, polymer, and metal layers of the device must be resorbable within the biological environment opens a new avenue for research into materials for bioresorbable electronics[119, 505, 510–518]. Extensive research has been put into bioresorbable metals that can safely degrade in bodily fluids while maintaining their functionality during the device's operational period. However, from the manufacturing perspective, this condition may result in a limited number of viable metallization methods remaining available. **Figure 8(g)** illustrates the transient properties of a bioresorbable pacemaker, where the stimulating electrodes are made of molybdenum (Mo), a metal chosen for its controlled degradation rate and compatibility with biological tissues. Alongside Mo, other widely used biodegradable metals include magnesium (Mg), zinc (Zn), and tungsten (W). Each of these metals offers unique properties with different degradation rate and a careful material selection is needed for the optimization of the bioelectronics[481, 505, 510, 518–519].

In bioelectronics, encapsulation must not only protect the body from potential leakage currents or inflammatory responses but also safeguard the device itself from mechanical deformation and provide a fluidic barrier for extended use within the human body[520–522]. Encapsulation is particularly critical for crystalline silicon-based flexible electronics due to silicon's brittleness and sensitivity to applied strain. Given silicon's inherent fragility, a protection and stress-relief strategy are essential to ensure its functionality in flexible applications. To stabilize SiNMs in various deformative environments, careful consideration of their placement within the flexible electronics is required[491–492, 523–529]. For example, during bending, the inner layers of a device experience compressive strain, while the outer layers undergo tensile strain, creating a neutral mechanical plane where the applied strain is minimized. To reduce strain effects on crystalline silicon, many flexible electronic devices are designed with the careful selection of encapsulation materials and thickness to position the SiNM near this neutral mechanical plane[111].

Moreover, encapsulation or passivation layers can serve dual purposes by functioning as active components in silicon-based electronics, such as in strain or pressure sensing applications. For instance, **Figure 8(h)** illustrates a crystalline SiNM-based strain gauge transferred onto an air cavity for pressure detection[530]. In this design, the SiNM strain gauge is encapsulated within PLGA layers and positioned over the cavity, which deforms under applied pressure. This deformation induces strain across the silicon, resulting in changes in conductivity due to the modulated electrical properties of the silicon. Additionally, another SiNM is positioned on top of the PLGA layer, serving as a barrier encapsulation that not only protects the underlying device but also strategically modulates the location of the neutral mechanical plane within the device. **Figure 8(i)** presents a graphical diagram illustrating the shift of the neutral mechanical plane during the dissolution of the SiNM encapsulation. As the SiNM barrier, being the outermost layer, dissolves first in a biofluidic environment, its thickness decreases, causing the neutral mechanical plane to shift downward. This shift, in turn, alters the sensitivity of the silicon strain gauge. Since the neutral plane is largely determined by the material's thickness, adjusting the thickness and location of the Si strain gauge allows for fine-tuning of the sensitivity to the desired value. **Figure 8(j)** demonstrates this strategic design through analytical and simulated results, showing that the positioning of the Si strain gauge can control sensor sensitivity changes during the dissolution of the SiNM barrier encapsulation. Furthermore, it illustrates that by optimizing the location, stable sensor performance can be maintained during transient operation.

3.2 Device transfer process (backside etching)

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The flexible usage of crystalline silicon offers incomparable benefits over bottom-up fabricated silicon-based electronics, primarily due to its superior electrical properties and high carrier mobility[443]. However, traditional substrate transfer processes which are characterized by a generic sequence of SiNM release, pick-up, and transfer printing, have struggled to fully leverage such advantages of crystalline silicon[135]. The conventional substrate transfer method typically begins with etching a sacrificial layer beneath the functional crystalline silicon membrane for its release from the mother wafer. During this etching process, the active silicon area must be patterned and exposed to strong chemicals like HF, TMAH, or KOH[220, 222, 226, 489–490, 531]. Although silicon exhibits significant resistance or may be intentionally passivated against these chemicals, other fabricated components, including metals and oxides, are less compatible, thereby limiting the transfer to the silicon membrane alone. Following the progression of the aforementioned sections, the thinned and doped silicon layer, transferred onto a flexible substrate, undergoes the flexible manufacturing cycle, eventually achieving the final device configuration. Such substrate transferring approaches significantly limit the range of manufacturing options at hand, primarily due to constraints related to the thermal budget of the post-transfer environment, and often result in inferior device performance compared to devices entirely fabricated on the wafer[135, 488].

On the other hand, the device transfer method, also referred to as the back-etching method, offers significant advantages over the substrate transfer method[167, 532]. Unlike the traditional approach, the back-etching method allows for the complete fabrication of the device on the wafer before transferring it to a flexible substrate (**Figure 9(a)**), which enables the utilization of high-temperature processes and precise fabrication techniques. The process begins with coating a bonding layer, typically made of materials such as photoresist, Kwik-Sil, or PI, onto the entire device. The backside of the SOI wafer, with a silicon thickness exceeding 500 μm, is then etched. While wet etching, such as using KOH or TMAH solutions, can efficiently remove large volumes of silicon, these solutions can also affect non-silicon materials, making them unsuitable for flexible transfer processes. In this context, dry etching techniques are predominantly employed for etching the backside silicon carrier layer. Several etching techniques are available. One option is using RIE with gases like SF_6 or CF_4, though this method tends to have a low etch rate and is inefficient for etching silicon thicknesses in the range of several hundred microns. A more efficient approach is inductively coupled plasma reactive ion etching (ICP-RIE), which utilizes SF_6 gas and exploits magnetic-induced plasma to increase the etching speed. However, it still requires precise etch stopping to ensure the desired thickness and minimize surface damage[167, 532] For applications involving a BOX layer for flexible electronics, the XeF_2 dry etch technique is a viable alternative[84]. XeF_2 etches silicon isotropically with high selectivity and can be used with the BOX layer as an etch stop, effectively preserving its integrity[217].

Thermally grown SiO_2 has been shown to exhibit superior barrier performance compared to SiO_2 deposited through methods such as sputtering, evaporation, or PECVD[178, 231, 377, 404, 532]. Electrical impedance spectroscopy (EIS) was performed on various SiO_2 encapsulation layers in phosphate-buffered saline (PBS), as seen in **Figure 9(b)**[166]. The results indicated that the t-SiO_2 layer demonstrated an outstanding, nearly perfect capacitor-like response across a broad frequency domain. In contrast, PECVD and evaporated SiO_2 exhibited relatively lower impedance in the lower frequency domain. This highlights the superior barrier properties of the dense and highly uniform t-SiO_2 encapsulation, which effectively prevents leakage through pinholes or direct permeation. Also, an electrical calcium test was performed to compare the long-term water barrier performance of t-SiO_2 with sputtered and PECVD SiO_2, all with the same thickness of 500 nm (**Figure 9(c)**)[165]. The water molecules penetrated the oxide barrier of the sputter and PECVD SiO_2 after only 133 minutes and 230 minutes, respectively, leading to the oxidation of the calcium. However, the calcium sample encapsulated with t-SiO_2 remained protected, with the oxide barrier effectively preventing moisture ingress and maintaining the sample's initial state even after 300 minutes. An areal encapsulation test with a multiplexed active electrode array was demonstrated through a soaking test in PBS at 70 °C (**Figure 9(d)**)[166]. With the 252 sensing sites, the yield of survival in PBS sustained a high yield over 10 days. This result showed that the t-SiO_2 has promising applicability in various implantable bioelectronics, including capacitively coupled electrodes and chronic electronics.

Building on the advantages of the t-SiO_2 barrier, there has been active research into utilizing crystalline silicon-based flexible bioelectronics for chronically implantable devices. Leveraging well-established silicon manufacturing processes and device transfer techniques, researchers have successfully demonstrated long-term neural recording using high-performance multiplexed electrode arrays. For example, a conductively coupled active array for high spatial resolution mapping of neural signals was developed and encapsulated with a t-SiO_2 layer (**Figure 9(e)**)[187]. The active electrode array was fabricated by first manufacturing NMOS source-follower amplifiers on an SOI wafer, followed by bonding with a flexible PI substrate. After the backside wafer etching process, the t-SiO_2 BOX layer served as an insulating interface between the tissue and the electronics. **Figure 9(f)** illustrates how the t-SiO_2 insulating barrier enabled leakage-free and chronic use of the underlying MOSFETs. This feature is particularly important in active electronics, where high-resolution mapping and low crosstalk noise are crucial for effective neural recordings. The integration of t-SiO_2 encapsulation ensures the stability and reliability required for long-term implantation in bioelectronics, making it a key component in the development of advanced neural interfaces and other implantable technologies. From an accelerated lifetime test conducted in 95 °C PBS, the MOSFETs demonstrated stable and high performance over 30 hours (**Figure 9(g)**). Considering that the thickness of the t-SiO_2 in this experiment was 1 μm, these results indicated that this stable neural interface can potentially operate for an extended, near-permanent duration.

In addition to its role as a biofluid barrier, the t-SiO_2 layer can also serve as a dielectric layer for capacitive coupling

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between the tissue and the electrodes when using the device transfer method. A capacitively coupled neural interface array, featuring a 28 × 36 electrode array, illustrates the scalability achievable through on-wafer manufacturing (**Figure 9(h)**)[533]. Furthermore, by fabricating the electrode arrays encapsulated by double-sided t-SiO_2 layers, the device's lifetime is enhanced to a scale of years. This capacitive coupling method highlights the advantages of the t-SiO_2 barrier, as it provides complete coverage compared to conductively coupled electrode arrays, which require a via patterning for electrical pads.

Along with approaches to integrate t-SiO_2 into flexible bioelectronics as a reliable and multi-functional biofluid barrier, recent studies have presented results on enhancing device stability through double-sided encapsulation, where a layer of t-SiO_2 is applied both at the top and bottom of the device. Multiple manufacturing strategies have been attempted for this purpose. **Figure 9(i)** shows the SOI-based wafer bonding procedure used by Shin *et al.* for a double-sided encapsulation of a bioresorbable intercranial pressure and temperature sensor system[534]. The authors implemented double-sided t-SiO_2 encapsulation by bonding two SOI wafers and subsequently performing back-etching of the handle wafer, to utilize the t-SiO_2 of each BOX layer. Alongside the double-sided t-SiO_2 encapsulation, the bioresorbable functionality of t-SiO_2 when produced in the form of ultrathin films was also leveraged in the research. Based on the fact that the malfunction of t-SiO_2 encapsulation is caused by the hydrolysis reaction of the oxide itself rather than by water permeation, the oxide layer was adopted in the proposed bioresorbable sensing system. The researchers demonstrated the clinically stable operation of the sensing system over a week and confirmed the clean bioresorption of the device afterward. **Figure 9(j)** shows the complete hydrolysis of the sensor device, composed of stacked layers of SiNM and t-SiO_2, after 80 hours of accelerated dissolution in PBS at 95 °C. By proper Arrhenius scaling with material property considerations, the given results correspond to a timescale of approximately 195 days at the range of biological temperatures around 37 °C.

3.3 Perspective

3.3.1 Perspective for substrate transfer process

Optimizing silicon etching in substrate transfer processes

The substrate transfer process begins with one of the most critical and challenging steps: silicon etching. This phase is foundational because it not only shapes the silicon according to the desired design but also significantly influences the success of the subsequent transfer and integration into functional devices[77, 135]. The precision and effectiveness of silicon etching are paramount, as any inaccuracies can lead to defects such as surface roughness, irregular patterns, or incomplete separation. These defects can compromise device performance, leading to issues such as poor adhesion to the substrate, electrical inefficiencies, or mechanical failures during device operation[535]. Therefore, optimizing the etching process is not just about achieving the correct dimensions and patterns but also about ensuring that the silicon maintains its structural integrity and desired properties throughout the entire manufacturing process. Advanced monitoring and control techniques during etching are crucial to minimize these risks and to ensure that the resulting silicon layers are both high-quality and fit for their intended bioelectronic applications.

Silicon etching can be broadly categorized into isotropic and anisotropic methods, each with distinct mechanisms and applications. While isotropic etching uniformly removes silicon in all directions, anisotropic etching selectively targets specific crystallographic planes, enabling the creation of highly precise, angular features that are essential for complex device architectures. However, the selection between these techniques is not straightforward and depends heavily on the specific requirements of the application, including the desired feature resolution, depth, and the material's compatibility with subsequent processing steps.

A critical consideration during silicon etching is the presence of multiple materials within the layered structure, such as metals, oxides, and other dielectrics[536–537]. The importance of etch stops and selective etching becomes paramount in this context. Selective etching allows for the precise removal of silicon without damaging adjacent materials, preserving the integrity of the multilayer structure. This is particularly important when working with complex devices where metals and oxides are present, as these materials often require different etching chemistries and conditions. The choice of etching technique must ensure that these materials remain unaffected, maintaining the overall performance and reliability of the device.

Wet etching techniques, such as those involving KOH, TMAH, hydrofluoric/nitric/acetic acid (HNA), and ethylene diamine pyrocatechol (EDP), offer various advantages but also present challenges. For instance, while KOH and TMAH are excellent for producing sharp, well-defined features due to their anisotropic nature, they require careful control over etching parameters to avoid unwanted undercutting or surface roughness, which could negatively affect the performance of the final device[222, 243]. In scenarios where metals and oxides are involved, it is crucial to ensure that the etching process does not inadvertently remove or damage these layers. Similarly, HNA, with its isotropic etching characteristics, is valuable for achieving smooth, rounded surfaces but may not be suitable for applications requiring high aspect ratio structures.

In contrast, dry etching methods like RIE provide high resolution and are better suited for achieving deep, vertical sidewalls[538]. However, they come with their own set of challenges, such as the potential for plasma-induced damage, issues with selectivity when etching through multilayer structures, and the need for precise control over etch stop layers to prevent over-etching[490]. The choice of etching gases (e.g., SF_6, CF_4, CHF_3, Cl_2) further complicates this process, as each gas offers different benefits and limitations in terms of etching rate, selectivity, and compatibility with the underlying materials.

In summary, the selection and application of appropriate etching techniques are critical to the success of the substrate transfer process in silicon-based bioelectronics. Beyond simply

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choosing between isotropic and anisotropic methods, engineers must also consider the potential pitfalls of each technique, such as surface roughness, undercutting, plasma damage, and the challenges posed by etching in the presence of multiple materials like metals and oxides. Developing strategies to mitigate these risks, such as using etch stop layers and ensuring selective etching, is essential. This often involves a combination of precise process control, advanced material characterization, and the use of complementary etching methods to achieve the desired outcome. Through careful planning and execution, it is possible to optimize the etching process to produce high-performance, reliable silicon devices suitable for a wide range of bioelectronic applications.

Considerations of the flexible substrate choice

The compatibility of the silicon membrane with various substrate materials is another critical consideration in the substrate transfer process. Different substrates, such as polymers, biodegradable materials, and stretchable materials, have unique properties, including thermal expansion coefficients, chemical resistance, and mechanical flexibility, which can affect the performance and durability of the transferred silicon. Mismatches in thermal expansion, for example, can lead to warping, delamination, or cracking during processing or operation, especially when subjected to varying environmental conditions. Additionally, chemical interactions between the substrate and silicon, or the adhesives used during the process, can result in degradation or loss of functionality over time. The chemical properties of the substrate also impose limitations on subsequent fabrication techniques after substrate transfer. For instance, widely used bioresorbable materials like poly(vinyl alcohol) (PVA) pose challenges as flexible substrates due to their reactivity with water, which restricts further fabrication processes involving water. To address this issue, research has explored the use of PVA substrates by employing a pick-up process for transferring silicon devices onto the PVA film, rather than a stamping process, thereby eliminating the need for additional manufacturing steps[539]. Similarly, ongoing research should focus on developing and characterizing new substrate materials that are more compatible with silicon, particularly those capable of withstanding the rigors of the transfer process and the operating environment. Exploring surface modification techniques or intermediate layers that can enhance adhesion and reduce thermal or chemical incompatibilities will also be important. Furthermore, expanding the range of compatible substrates, including those that are biodegradable or stretchable, will open up new possibilities for applications in bioelectronics and wearable technologies.

Challenges and future directions in substrate transfer processes

The substrate transfer process presents several critical challenges that must be addressed to enable successful scaling and commercialization. Key concerns include maintaining uniformity and yield, achieving scalability, ensuring material compatibility, and guaranteeing long-term stability while minimizing defects[535]. Overcoming these challenges requires a deep understanding of materials science and engineering, coupled with ongoing research to refine techniques and develop innovative solutions.

Achieving uniform thickness and consistent material properties across large-area substrates is one of the primary challenges in substrate transfer processes. This uniformity is crucial for ensuring that all regions of the silicon membrane perform consistently, which is particularly important in applications where precision is critical, such as in bioelectronics. However, maintaining this uniformity is difficult due to the inherent complexities of the transfer process, including potential variations in adhesion, substrate surface roughness, and the handling of ultra-thin silicon layers. Even slight deviations in thickness or material composition can lead to significant performance discrepancies, resulting in low device yield. The variability in the process can introduce defects such as thickness non-uniformity, wrinkles, or even cracks, which compromise the integrity and functionality of the transferred membranes. To overcome these challenges, further research is needed to refine the transfer techniques, possibly through the development of advanced monitoring systems that ensure real-time correction of deviations, and the exploration of new materials or adhesives that provide more consistent outcomes. Additionally, optimizing the deposition techniques and post-transfer processing methods could help achieve higher uniformity and yield, making the process more commercially viable.

Scaling up the substrate transfer process from laboratory settings to industrial-scale production presents significant challenges. Techniques that are successful at the small scale often encounter difficulties when applied to larger areas or higher volumes. Issues such as alignment precision, uniform application of forces during transfer, and maintaining the integrity of large-area silicon membranes become more pronounced as the process scales up[236, 540]. Furthermore, the equipment and techniques used in the lab may not be suitable for the continuous or high-throughput processes required in industrial settings. This scalability issue limits the widespread adoption of these technologies in commercial applications. To address this, research into high-throughput methods such as roll-to-roll transfer, which allows for continuous processing of flexible substrates, is essential. Such methods must be refined to handle the delicate nature of silicon membranes while ensuring precision and uniformity. Additionally, developing scalable methods for quality control, such as inline inspection systems that can detect and correct issues during the transfer process, will be critical for enabling the mass production of high-quality flexible silicon devices.

Ensuring the long-term stability of transferred silicon membranes on flexible substrates is a significant challenge, particularly for applications that involve prolonged use or exposure to harsh environments. Over time, factors such as humidity, temperature fluctuations, mechanical wear, and biological interactions (in the case of implantable devices) can degrade the performance of these devices[522]. For instance, repeated mechanical stress from bending or stretching can lead to fatigue in the silicon membrane or the substrate, resulting in

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cracks or delamination[541]. Similarly, exposure to moisture or reactive chemicals can lead to corrosion or weakening of the adhesive bonds, ultimately compromising the device's functionality. Addressing these challenges requires a multifaceted approach. Research should focus on developing more durable materials and adhesives that can maintain their integrity over time, even under extreme conditions. Additionally, protective coatings or encapsulation techniques that shield the silicon and substrate from environmental factors could extend the lifespan of these devices. Advanced modelling and testing methods to predict long-term performance and identify potential failure points before they occur will also be crucial for improving the reliability of these systems.

Minimizing defects during the substrate transfer process is crucial for the reliable operation of silicon-based devices[535]. Defects such as cracks, voids, or particulate contamination can significantly impair the performance of the silicon membrane, leading to electrical failures, reduced mechanical strength, or poor device yields. These defects often arise from the handling and processing of ultra-thin silicon layers, which are highly susceptible to damage. In particular, manual transfer processes, which are commonly used due to their accessibility, can exacerbate issues such as misalignment and uneven stress distribution.

To address these limitations, scalable methods like roll-to-roll (R2R) transfer printing have been explored. R2R techniques offer an automated and high-throughput alternative, integrating alignment mechanisms to minimize defects while ensuring precise placement of devices over large areas. While manual methods are suitable for small-scale applications, R2R processes represent a promising direction for improving scalability and manufacturing efficiency. For example, Choi *et al.* employed roll transfer to apply a Si thin-film transistor (TFT) layer and LED array, ensuring they were well aligned for integration. To ensure proper alignment of each transistor, this study suspended the components using anchors at the edges[542]. Additionally, Sharma *et al.* presented a load-controlled roll transfer method that prevents misalignment of transferred thin transistor arrays[543].

Despite these advancements, it is important to acknowledge that the defect-related challenges associated with flexible electronics can lead to performance limitations compared to traditional rigid devices. Rigid devices, being inherently more robust and less susceptible to mechanical deformation, typically exhibit higher reliability and stability under demanding conditions. Furthermore, rigid substrates are less prone to defects such as cracks or delamination during fabrication, resulting in higher device yields and more consistent performance metrics. Flexible devices, while offering advantages in adaptability and lightweight design, require further improvements in transfer and handling techniques to achieve comparable performance to their rigid counterparts. Continued innovation in defect detection, prevention, and scalable manufacturing processes will be essential for bridging this gap.

Overcoming the challenges associated with substrate transfer processes is essential for advancing research in flexible silicon-based devices. Addressing key issues such as maintaining uniformity and yield, achieving scalability, ensuring material compatibility, guaranteeing long-term stability, and minimizing defects will require continued research and innovation. By refining existing techniques and exploring new approaches, the scientific community can push the boundaries of flexible electronics, enabling the development of more reliable and high-performance devices for applications in bioelectronics, wearable technologies, and beyond.

3.3.2 Perspective for device transfer process

Perspective on SiO_2 encapsulation in device transfer processes:

Thermally grown SiO_2 is a highly effective encapsulation material, offering excellent protection against moisture, ions, and contaminants due to its high density and uniformity. It also serves as an outstanding electrical insulator, ensuring long-term stability for bioelectronic devices, particularly those intended for implantation[166, 525, 544]. These properties make SiO_2 ideal for protecting transferred devices in demanding environments. However, a critical limitation of the current use of t-SiO_2 in device transfer processes is that it typically encapsulates only one side of the silicon membrane. While this single-sided encapsulation provides robust protection for the covered surface, it leaves the other sides-particularly the opposite face and the edges-vulnerable to ion and moisture ingress once the device is implanted. In a biological environment, this exposure can lead to the diffusion of water, ions, and other small molecules through the unprotected areas, gradually degrading the device's performance. Over time, this degradation can manifest as electrical instability, loss of functionality, or even complete device failure.

To address this challenge, research must focus on developing all-around encapsulation techniques that can provide comprehensive protection to the entire device. This would involve not only covering the top surface with SiO_2 but also extending the encapsulation to the sides and bottom of the silicon membrane. Achieving such comprehensive encapsulation is crucial for preventing any pathway through which ions or moisture could penetrate the device.

One potential approach to achieving all-around encapsulation could involve multi-step processes where additional layers of SiO_2 or other protective materials are deposited post-transfer. Another avenue of research could explore the development of novel encapsulation techniques that allow for conformal coverage of the entire device, including the sides and edges. Furthermore, integrating SiO_2 encapsulation with other barrier materials that complement its properties could enhance the overall protection, ensuring that no part of the device remains exposed to the corrosive biological environment. Since all-around encapsulation using t-SiO_2 has never been significantly explored, there is a significant opportunity for additional

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research and the development of innovative process technologies in this area.

In conclusion, while t-SiO_2 provides exceptional encapsulation for one side of transferred devices, there is a pressing need for advancements in all-around encapsulation methods to ensure the long-term reliability and performance of bioelectronic implants. By addressing this gap, future research can significantly improve the durability and effectiveness of flexible silicon-based devices, paving the way for safer and more reliable bioelectronics applications.

4. Bioelectronics applications

As introduced, the integration of single crystalline silicon into bioelectronics is made possible through sophisticated on-wafer processing and transfer techniques. These methods allow for the precise modulation of silicon's properties and the use of appropriate materials and processes tailored to the device's specific functions and objectives. Devices produced through transfer processes can be categorized into passive types, such as resistors and electrodes, and active types, such as diodes and transistors. Crystalline silicon-based bioelectronics exhibit exceptional inherent characteristics, as highlighted in **Table 1**, making them highly suitable for various applications.

Its ability to modulate properties, such as high piezo-resistance and TCR, enables the creation of highly sensitive devices. Silicon's inherent reliability, high-temperature stability, and biocompatibility make it an ideal candidate for bioresorbable implants, which are crucial for transient medical applications. Furthermore, its high electron mobility is advantageous for creating efficient electronic devices. As a result, researchers have been able to leverage silicon's unique characteristics to develop high-performance bioelectronic systems that are both effective and adaptable for various biomedical applications.

In the realm of electrophysiological recording, a fully bioresorbable neural implant system was developed, utilizing silicon's outstanding properties to enable both electrical recording and optogenetic stimulation[124]. **Figure 10(a)** illustrates the dissolution mechanism of silicon. As shown in **Figure 10(b)**, the system integrates a biodegradable Mo/Si electrode array with a flexible PLGA waveguide, engineered to reduce optical losses and minimize artifacts. This sophisticated design, facilitated by advanced fabrication techniques such as photolithography and RIE, has been validated in chronic implantation studies, demonstrating reliable neural monitoring in transgenic mice (**Figure 10(c)**). **Figure 10(d)** demonstrates that the silicon-based system not only performs efficiently but also biodegrades entirely, underscoring its potential in neurotechnology for both research and therapeutic applications. For thermal detecting applications, Sang *et al.* developed an ultrathin, highly sensitive Au-doped SiNM temperature sensor array, effectively overcoming the limitations of traditional silicon. As represented in **Figure 10(e)**, the novel gold doping process enhances the sensitivity of the SiNM, resulting in a TCR significantly higher than that of conventional sensors[352]. The serpentine mesh structure allows the sensor to conform closely to the skin, providing accurate and stable temperature monitoring even in dynamic environments (**Figure 10(f)**). **Figure 10(g)** highlights how this advancement positions silicon-based sensors as vital tools for precise thermal detection, with implications for medical diagnostics and chronic disease management.

Porosity-based heterojunctions in p-type silicon were employed to advance optoelectronic stimulation, enabling leadless and non-genetic modulation of biological tissues[551]. They utilized the photoelectronic properties of silicon (**Figure 10(h)**), while forming porous/non-porous heterojunctions (**Figure 10(i)**), created via stain etching and high-power oxygen plasma treatment, to facilitate efficient photovoltaic stimulation without requiring complex instrumentation. The researchers implemented a biocompatible diode-like device by a straightforward process of altering the physical properties of silicon, utilizing its compatibility with finely tunable manufacturing techniques. The form factor of the thin and flexible silicon membrane, combined with the porosity-induced soft biointerface, allowed the device to adhere well to various biological tissue surfaces without the need for additional adhesives or suturing (**Figure 10(j)**). In vivo experiments confirmed the therapeutic efficacy of this approach, demonstrating successful sciatic nerve stimulation in a rat model with nerve injury (**Figure 10(k)**). Optical stimulation with pulsed lasers of 532 nm and 808 nm induced an action potential, leading to associated lower limb movement. The accompanying graph illustrates the action potential amplitude generated by the irradiated near-infrared laser as a function of pulse length, along with the corresponding maximum leg displacement. This finding underscores the potential of such silicon-based bioelectronics for therapeutic applications while minimizing discomfort and muscle fatigue.

A novel biodegradable and self-deployable electronic tent interface was developed for cortical interfacing[476]. As shown in **Figure 11(a)**, this study utilized the electrical changes observed in silicon when subjected to mechanical deformation. Utilizing SiNM doped and patterned on SOI wafers, the device is capable of significantly expanding post-implantation, covering a large area of the brain cortex (**Figure 11(b)**). **Figure 11(c)** demonstrates the integration of the silicon-based strain sensor and various other functional sensors and components in a mesh structure. As illustrated in **Figure 11(d)**, the silicon-based strain sensor embedded within the system enables the acquisition of various biomechanical signals, such as brain pressure, further enhancing its utility. This self-deployable nature reduces surgical complications and allows for the integration of additional functionalities, such as microelectromechanical systems. The biodegradability of the device minimizes the risks associated with implantation and removal, marking a significant advancement in brain-computer interface technologies. A bioresorbable silicon-based neurochemical analyzer was developed, integrating 2D materials like MoS_2 and WS_2 with crystalline silicon for wireless monitoring of neurotransmitters in the brain (**Figure 11(e)**)[545]. As depicted in **Figure 11(f)**, the device, fabricated through t-SiO_2-assisted selective doping of SiNMs, is capable of sensitive and selective detection of

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neurochemicals such as dopamine. **Figure 11(g)** highlights how the integration of 2D materials enhances the system's performance, making it suitable for diagnosing and treating neurodegenerative diseases. The fabrication process involves the transfer of the SiNM onto a biodegradable substrate, with careful selection and integration of materials being critical for reliable long-term performance. This study represents a significant step towards fully implantable, bioresorbable silicon-based neurochemical monitoring systems. A flexible silicon transistor array was developed for long-term cardiac electrophysiology, exemplifying silicon's potential in bioelectronics by leveraging its excellent electrical performance and high mobility, as illustrated in **Figure 11(h)**[162]. As shown in **Figure 11(i)**, the device, fabricated on SOI wafers using conventional photolithography and RIE, utilizes capacitive coupling to record electrical activity without direct metal contact, thereby reducing current leakage risks. The crystalline silicon-based transistors were transferred onto a flexible Kapton substrate, enabling high-density cardiac activity mapping (**Figure 11(j)**). This system's biocompatibility and long-term stability represent significant advancements in cardiac monitoring, with future efforts focused on optimizing foreign-body response and enhancing in vivo monitoring capabilities.

Silicon-based bioelectronics, particularly in flexible and bioresorbable applications, face several potential failure modes that can compromise their longevity and performance[571–572]. Mechanical stress and strain during operation may lead to issues such as delamination, cracking, or deformation, reducing device functionality[573]. Encapsulation degradation, especially in bioresorbable systems, can expose sensitive components to environmental factors, accelerating device failure[130–131, 574]. To address these challenges, researchers have explored strategies such as improved encapsulation designs using multilayer coatings, mechanical reinforcement through hybrid materials, and optimized transfer techniques to minimize stress during fabrication and implantation[522, 525, 575]. While the advancements in silicon-based flexible electronics for biomedical applications are remarkable, it is essential to address safety and ethical issues from both hardware and software perspectives[576–577]. From the hardware standpoint, the long-term biocompatibility of these devices must be assessed to prevent risks such as tissue inflammation, foreign-body responses, or toxicity from degradation products[127]. On the software side, safeguarding user safety against potential breaches of private and sensitive data is paramount[578–579]. Ensuring robust safety measures and ethical guidelines in such aspects is critical to fostering trust, enhancing user confidence, and supporting the responsible integration of these technologies into clinical and research environments[128–129].

5. Conclusion and outlook

The integration of crystalline silicon into bioelectronics has revolutionized the field, enabling the development of high-performance, flexible, and bioresorbable devices that interact seamlessly with biological systems. This review has provided a comprehensive exploration of the key processes and innovations that have made silicon an indispensable material in bioelectronics (**Figure 12**). From its historical role in the semiconductor industry to its current applications in next-generation medical technologies, silicon's unique properties-including exceptional electronic performance, chemical and optical properties, scalability, biocompatibility, and mechanical stability-continue to drive advancements in this dynamic field.

The transition of rigid silicon into flexible form factors has been achieved through sophisticated manufacturing processes, including on-wafer techniques like oxidation and doping, as well as advanced transfer printing methods that integrate silicon with flexible substrates. These processes have not only preserved silicon's superior electronic properties but have also unlocked new possibilities in wearable and implantable medical devices, transient electronics, and neural interfaces. The ability to fabricate devices that are both high-performing and adaptable to the soft, dynamic nature of biological tissues has opened new frontiers in medical diagnostics, therapeutic interventions, and real-time biological monitoring.

Looking forward, several challenges lie ahead in the further of silicon-based bioelectronics. One major challenge is enhancing the durability and functionality of flexible silicon devices, particularly in long-term implantable applications where biocompatibility and stability are critical. Additionally, the development of more cost-effective manufacturing techniques that can mass produce large-scale, high-quality SiNMs will be essential for the commercialization and widespread adoption of these technologies.

Key areas of future research and development include the industrialization and scaling up of transfer processes, addressing yield issues to enable large-area wafer-scale transfers. This will be necessary for producing bioelectronic devices suitable for clinical and commercial applications. Advances in BCIs and neural interfaces, leveraging the precision of silicon-based technologies, will open new possibilities in neuroprosthetics, cognitive enhancement, and the treatment of neurological disorders. Furthermore, the exploration of nanoscale processes will be essential for developing advanced bioelectronics. These processes will enable the fabrication of even smaller, more sensitive devices that can interact with biological systems at unprecedented levels of detail. Research into chip-less bioelectronics, which eliminates the need for traditional silicon chips, will also push the boundaries of what is possible in miniaturized medical devices. The development of extremely thin and small systems through layered stacking processes will allow for the creation of compact, multi-functional bioelectronics that can be seamlessly integrated into the body. These systems will benefit from the inherent properties of silicon while offering enhanced functionality and versatility. Additionally, the integration of controllable biodegradable devices, triggered by external stimuli, will enable new therapeutic strategies where devices can be modulated based on specific biological signals or conditions. In the realm of therapeutic bioelectronics, silicon-based devices will play a pivotal role in addressing cancer, neurodegenerative diseases, nerve regeneration, and chronic illnesses. These devices, designed for targeted therapy and precision medicine, will be

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crucial in delivering treatments with minimal side effects and maximal efficacy. Moreover, the development of low-power, high-efficiency systems will be essential to ensure the longevity and sustainability of implantable devices, reducing the need for frequent replacements and improving patient quality of life.

In conclusion, crystalline silicon remains a fundamental and irreplaceable material in the rapidly evolving field of bioelectronics. Its ability to be engineered into flexible, high-performance devices continues to offer unprecedented opportunities for innovation in healthcare and beyond. As research and development progress, silicon's role in bioelectronics is expected to expand, driving the creation of more sophisticated and versatile medical technologies that will lead to better patient outcomes and sustainable medical interventions.

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Figures

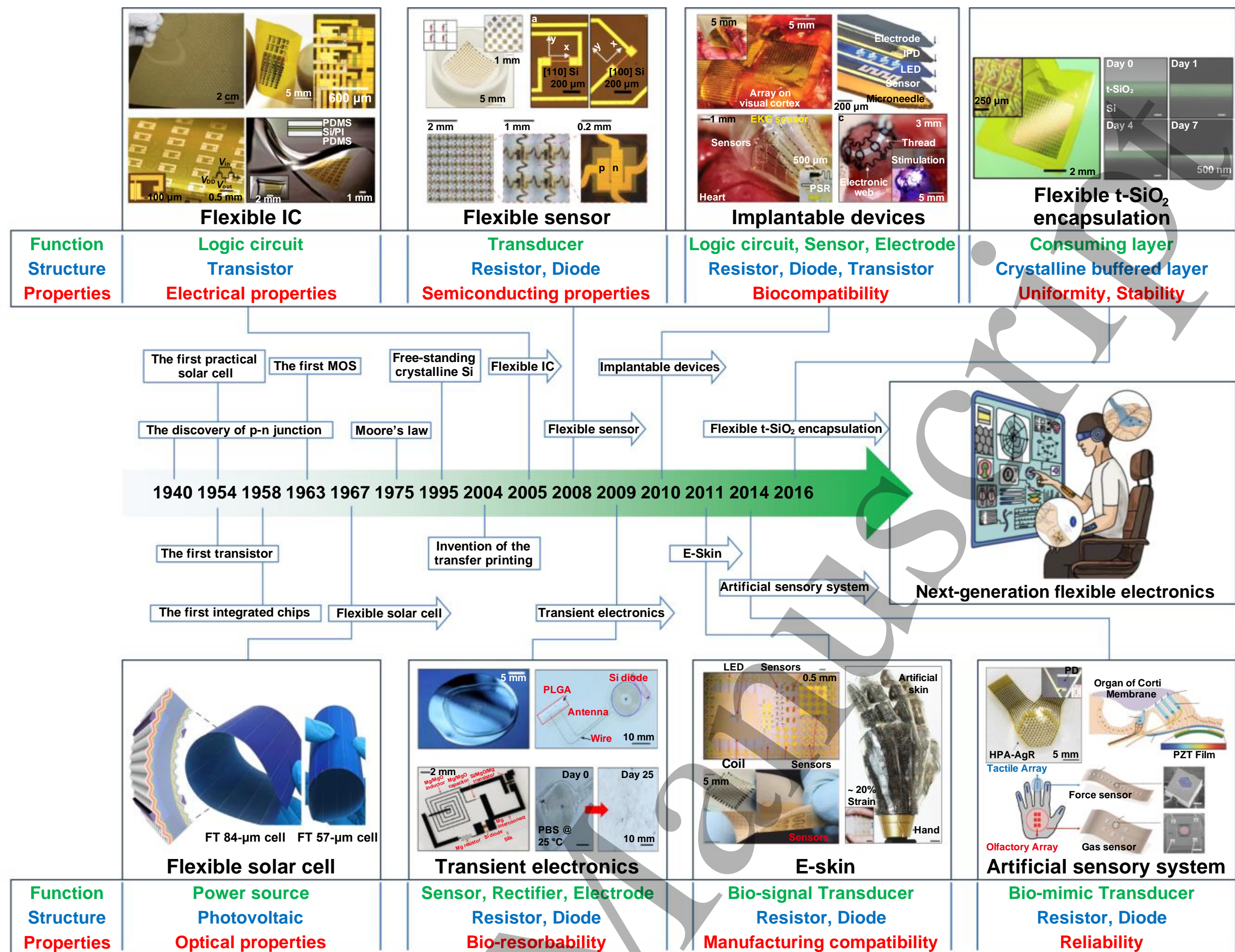

Figure 1. Crystalline silicon's journey from pioneering electronics to shaping the future of bioelectronics and beyond. Reproduced from [108]. CC BY 4.0. Reprinted with permission from [107]. © 2006 American Association for the Advancement of Science. Reprinted with permission from [106]. © Copyright 2008 IEEE. All rights reserved. Reprinted with permission from [92]. © 2008 American Association for the Advancement of Science. Reprinted with permission from [109]. © 2006 Springer Nature. Reproduced from [348]. CC BY 4.0. Reproduced from [115]. CC BY 4.0. Reprinted with permission from [112]. © 2011 Springer Nature. Reprinted with permission from [113]. © 2011 Springer Nature. Reprinted with permission from [116]. © 2013 American Association for the Advancement of Science. Reprinted with permission from [120]. © 2020 American Association for the Advancement of Science. Reprinted with permission from [123]. © 2024 Springer Nature. Reprinted with permission from [110]. © Copyright 2009 AIP Publishing. Reprinted with permission from [119]. © 2018 Springer Nature. Reproduced from [81]. CC BY 4.0. Reproduced from [114]. CC BY 4.0. Reprinted with permission from [117]. © 2018 Springer Nature. Reprinted with permission from [360]. © 2018 Springer Nature. Reproduced from [166]. CC BY 4.0. Reprinted with permission from [580]. © 2024 American Association for the Advancement of Science. Reproduced from [581]. CC BY 4.0. Reproduced from [582]. CC BY 4.0.

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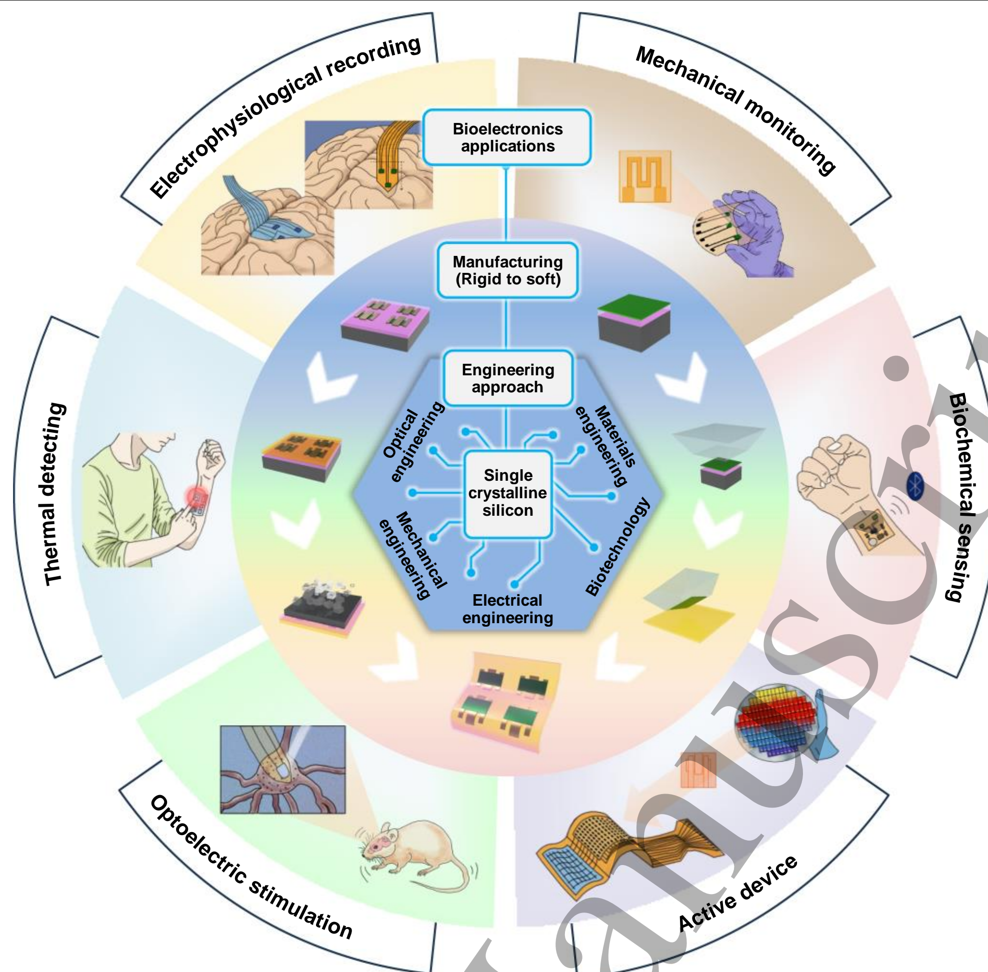

Figure 2. Multidisciplinary engineering strategies and manufacturing approaches for soft crystalline silicon bioelectronic devices.

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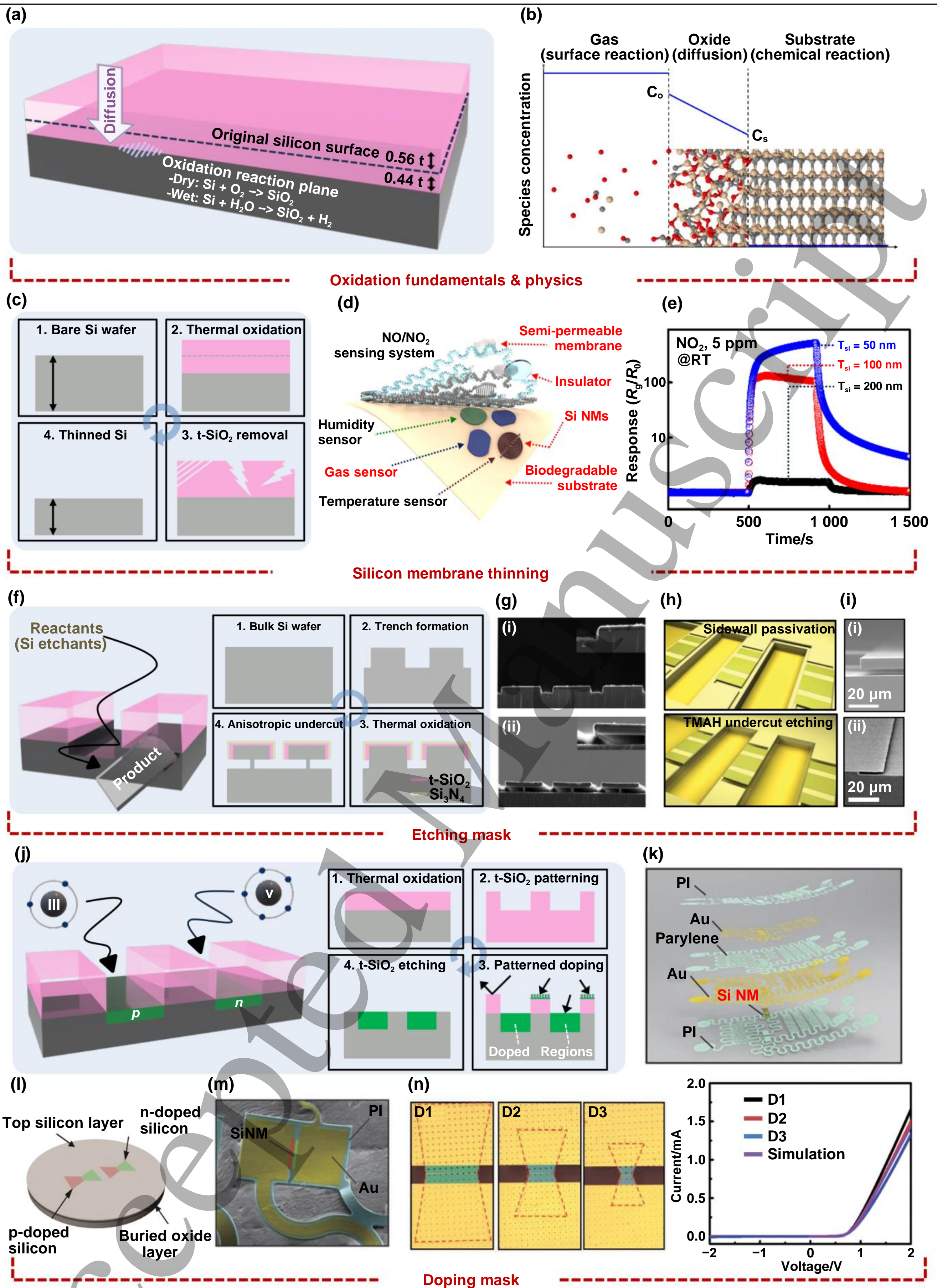

Figure 3. On-wafer processing of thermal oxidation and applications of t-SiO_2 in the manufacturing of silicon-based flexible bioelectronics. (a) Schematic illustration of the growth of t-SiO_2 on a silicon wafer through thermal oxidation, showing the quantitative ratio of consumed original silicon to formed t-SiO_2 layers above and below the original wafer surface. (b) A schematic of thermal oxidation kinetics based on the Deal-Grove model, correlating oxidation time to the t-SiO_2 thickness. Reproduced from [583]. CC BY 4.0. (c) A generic processing flow of silicon thinning through thermal oxidation, showing four sequential processing

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steps that may be repeated as needed. (d) Exploded view of the NO/NO_2 gas sensor system with SiNM as an active sensing component for gas, temperature and humidity. (e) Comparison of response results demonstrating the improvement in sensitivity and recovery depending on different thicknesses of the SiNM, obtained through thermal oxidation, highlighting the impact of optimizing the silicon thickness. (d) and (e) Reproduced from [204]. CC BY 4.0. (f) Conceptual illustration of t-SiO_2 used as a patterning mask layer during the silicon etching process (left). A generic processing flow of utilizing t-SiO_2 as an etching mask, particularly as a sidewall passivation layer for wet anisotropic etching of silicon, (right). (g) SEM images showing the trench sidewall passivation with a Si_3N_4/t-SiO_2 bilayer on a silicon wafer before performing anisotropic etching with KOH (top). SiNRs with thickness of 400 nm after the wet etching (bottom), both images contain a scale bar of 10 μm. Reproduced from [252]. CC BY 4.0. (h) Schematic representation of utilizing t-SiO_2 as a sidewall passivation layer (top) during the fabrication and release of ultrathin MOSFETs via TMAH anisotropic etching (bottom). (i) SEM images of the released silicon membranes with varying thicknesses of 800 nm (i) and 11 μm (ii). (h) and (i) Reprinted with permission from [158]. © Copyright 2013 AIP Publishing. (j) Conceptual illustration of t-SiO_2 used as a doping mask during the silicon doping process, along with a description of group III/V elements used for p-type/n-type doping of silicon (left). A generic processing flow of utilizing t-SiO_2 as a doping mask, applicable for both diffusion and ion implantation to dope the regions of interest (right). (k) Configuration of the SiNM-based PIN diode for an epidermal RF power harvester using t-SiO_2 as a doping mask. (l) Illustration showing the SiNM-based PIN diode fabricated on an SOI wafer. The n-/p-doped regions were defined by a repeated process of forming and removing a t-SiO_2 layer as the doping mask. (m) Colorized SEM image of the device transferred onto a skin replica. (n) Optical images of three PIN diode samples with varying physical dimensions (left) and the corresponding diode *I-V* curves. (k)-(n) Reproduced from [289]. CC BY 4.0.

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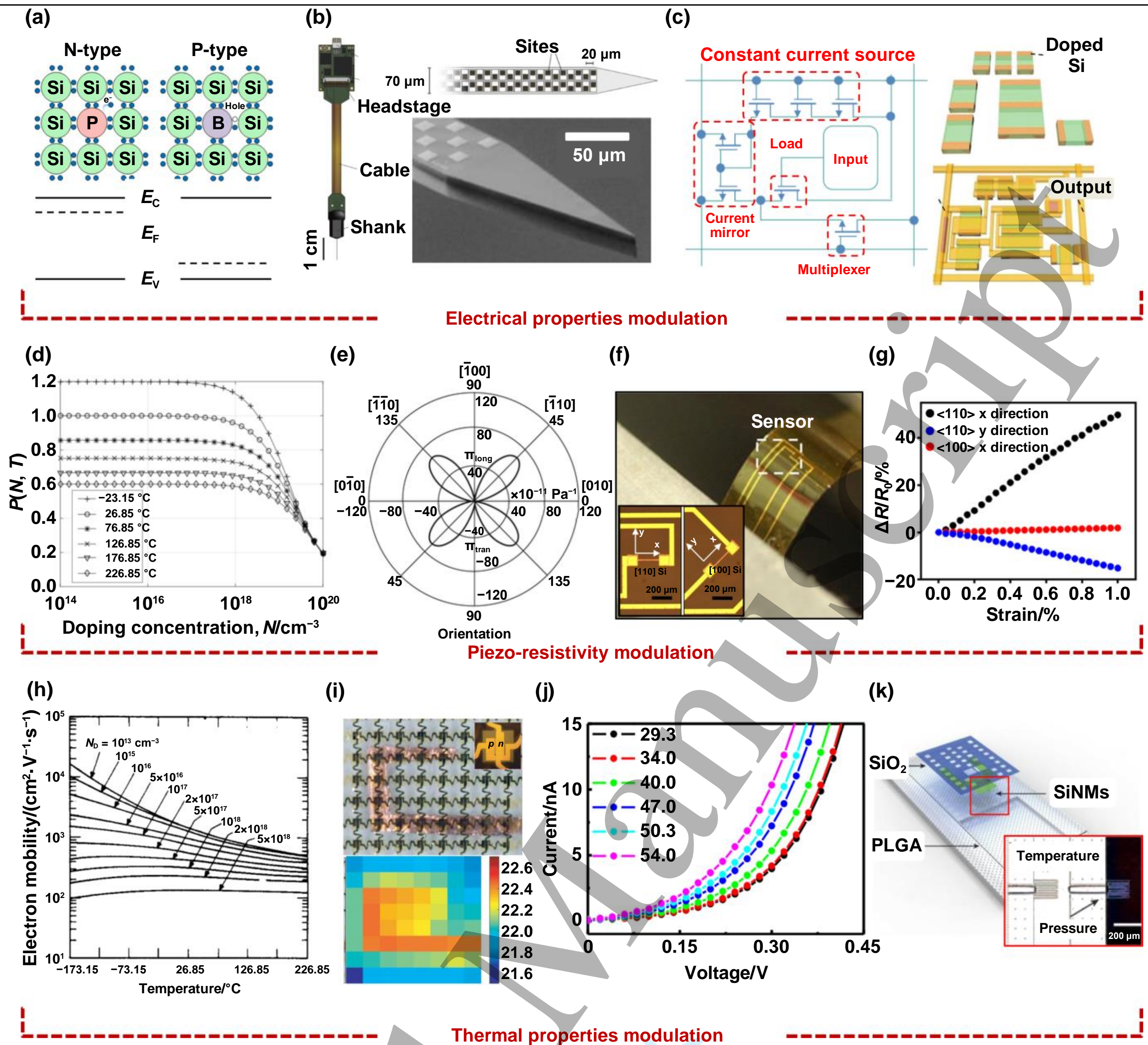

Figure 4. On-wafer processing of doping to modulate the electrical, mechanical, and thermal properties of silicon for flexible bioelectronics applications. (a) Illustration of n-type and p-type doping of silicon, showing the introduction of dopant atoms into the silicon lattice and their influence on electron and hole concentrations (top), along with the shift of the Fermi energy level in the energy band diagram (bottom). (b) Design of high-density neural recording electrodes, emphasizing the precision and scalability achieved through CMOS technology and doping processes, enabling stable and efficient neural signal acquisition. Reprinted with permission from [326]. © 2017 Springer Nature. (c) Schematic of analog circuits designed for electrophysiological signal processing in active-array flexible ECoG devices with doped silicon. Reprinted with permission from [111]. © 2010 American Association for the Advancement of Science. (d) Graph illustrating the effect of doping concentration on silicon's piezoresistive response, showing the relationship between charge carrier density and response to mechanical strain. Reproduced from [584]. © 2022 Springer Nature. (e) Polar diagram representing the crystallographic orientation dependency of silicon's piezoresistive coefficient, highlighting differences between [100], [110], and [111] orientations. Reprinted with permission from [333]. © 2012 Springer Nature. (f) Optical image of the multi-axis strain sensor using SiNMs with different crystallographic orientations of [110] and [100] (inset), demonstrating improved performance by leveraging [110] silicon's higher strain sensitivity. (g) Experimental results of strain response testing for [100] and [110] oriented SiNM, with [110] silicon demonstrating significantly greater sensitivity under longitudinal strain. (f) and (g) Reproduced from [348]. © CC BY 4.0. (h) Graph showing electron mobility in silicon at varying doping concentrations as a function of temperature, indirectly representing the Temperature Coefficient of Resistance (TCR) for lightly and heavily doped silicon. Reproduced from [350]. © CC BY 4.0. (i) Optical image (top) and temperature mapping demonstration (bottom) of a flexible temperature sensor array based on p-n diodes using SiNM. Reproduced from [115]. © CC BY 4.0. (j) Temperature dependency of flexible SiNM p-n diode. Reprinted with permission from [360]. © 2014 Springer Nature. (k) Illustration along with an inset of the optical image of the SiNM-based bioresorbable sensor for simultaneously monitoring intracranial pressure and temperature with high sensitivity and stability. Reprinted with permission from [118]. © 2016 Springer Nature.

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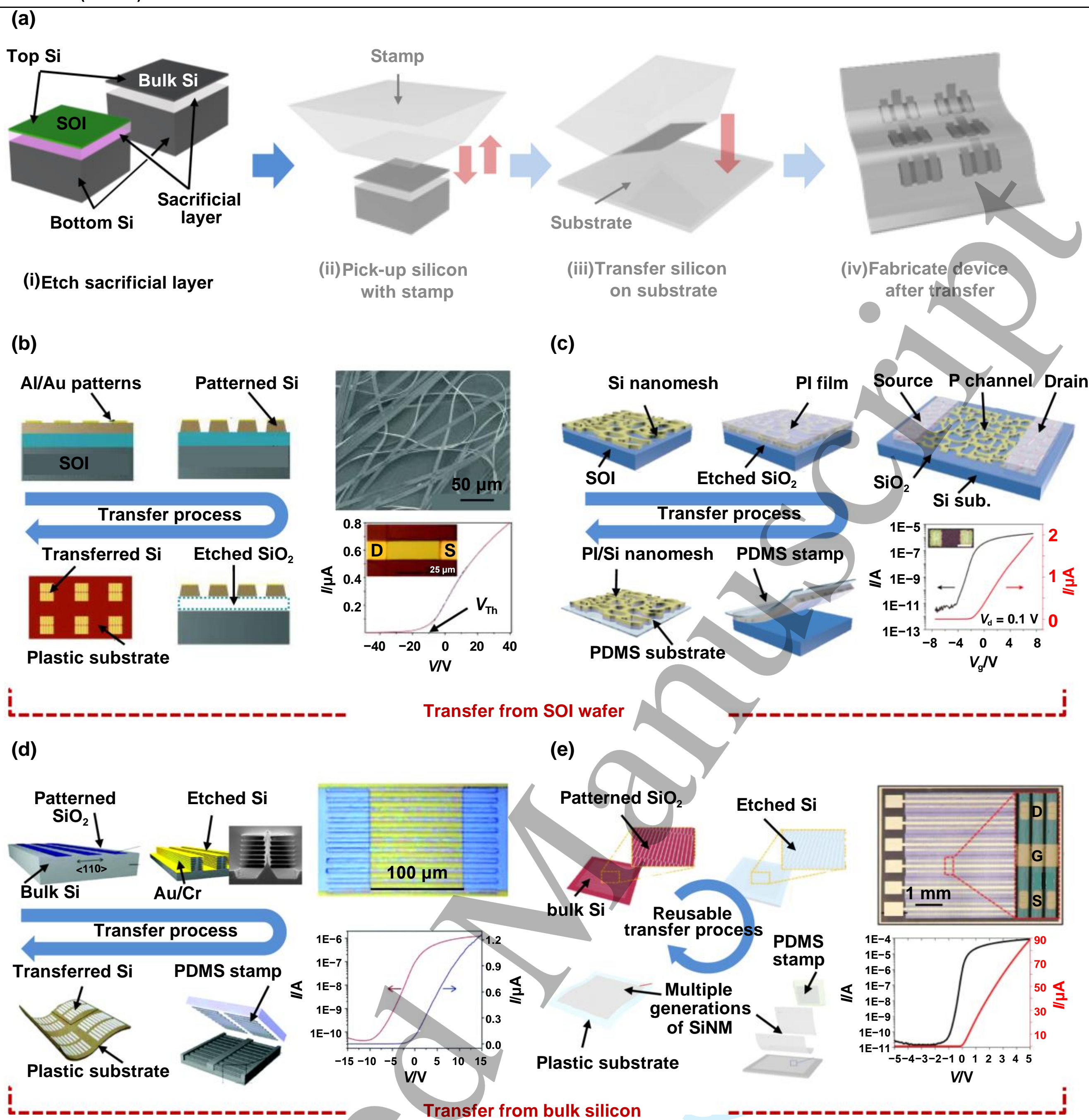

Figure 5. Comparative analysis of Silicon on Insulator (SOI) and bulk silicon-based substrate transfer processes for flexible bioelectronics. (a) Schematic of the substrate transfer process for silicon, with only the first step colorized (Step 1: etching the sacrificial layer; the BOX layer for SOI, the underlying silicon layer for bulk silicon). (b) Fabrication process (left) of thin-film transistors on flexible plastic substrates using single crystalline silicon bars and ribbons (right, top) transferred from SOI wafers, with the *I-V* curve measured from a single transistor cell (right, bottom). Reprinted with permission from [134]. © Copyright 2004 AIP Publishing. (c) Fabrication process (left) of stretchable electronics through the formation of nano-meshed SiNMs, transferred onto flexible substrates using a PDMS stamp to create a silicon nano-mesh transistor (right, top) along with the transfer curve of the sample in log (black curve) and linear (red curve) scale (right, bottom). Reproduced from [443]. © CC BY 4.0. (d) Fabrication process (left) of creating cost-efficient, large-scale production of silicon micro- and nanoribbons from bulk silicon, offering excellent electrical properties for flexible electronic applications. Optical images of MOSFETs utilizing the transfer printed Si ribbon array (right, top), with the transfer curve of a single transistor in log (black curve) and linear (red curve) scale (right, bottom). Reproduced from [73]. © CC BY 4.0. (e) Fabrication process (left) of creating ultrathin crystalline SiNM from bulk wafers, enabling multiple transfers and an optical image of 471 transistors (right, top) demonstrating the scalability of flexible silicon technologies along with the transfer curve of a single transistor in log (black curve) and linear (red curve) scale (right, bottom). Reproduced from [144]. © CC BY 4.0.

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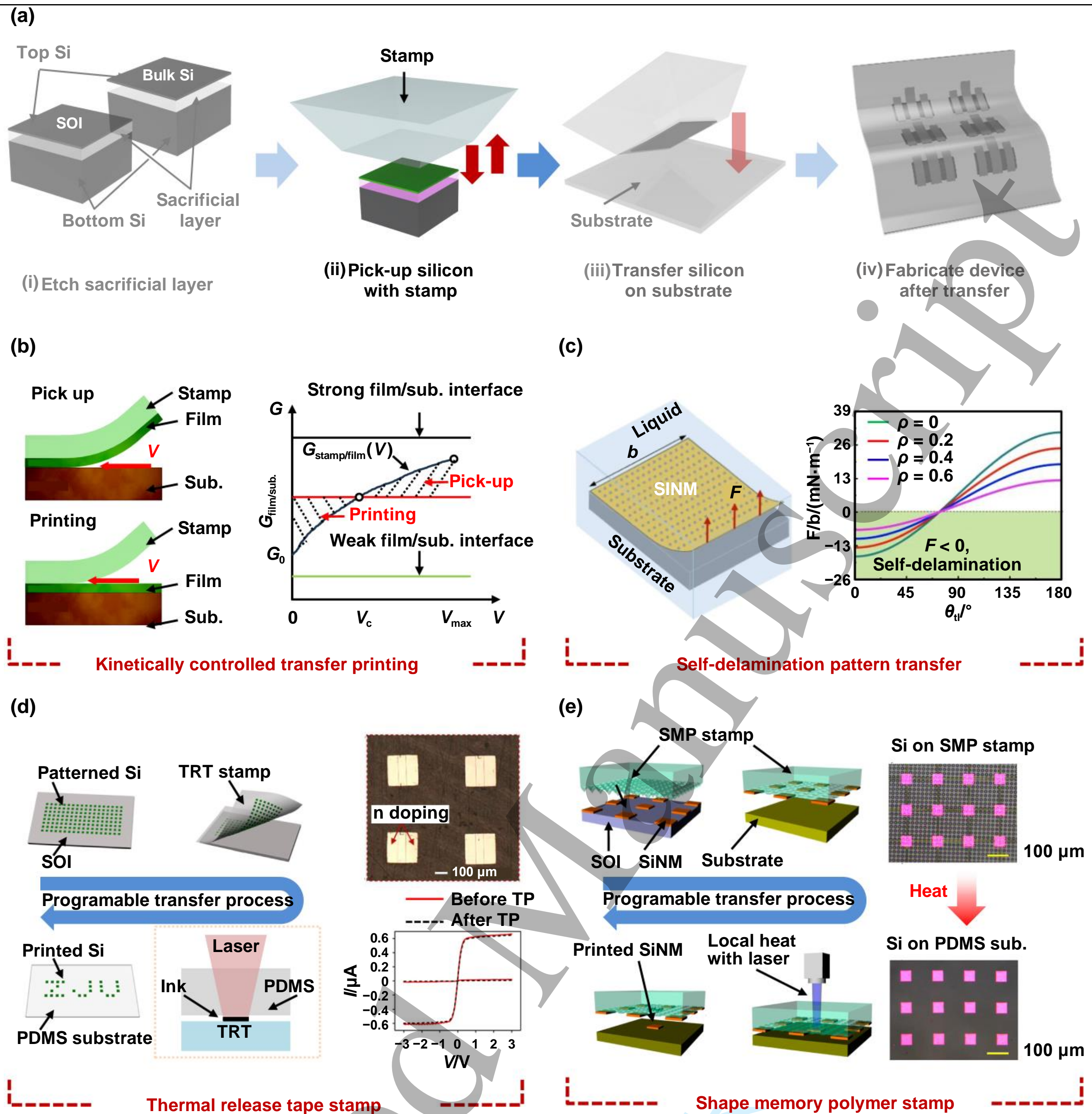

Figure 6. Analysis of pick-up mechanisms and diverse stamping approaches in the substrate transfer processes for flexible bioelectronics. (a) Schematic of the substrate transfer process for silicon, with only the second step colorized (Step 2: picking up the released silicon layer with an appropriate stamp). (b) Schematic of kinetically controlled transfer pick-up/printing process (left). The graph plots the critical energy release rate at both the interfaces of substrate/film and film/stamp against the peeling velocity (right). Reproduced from [460]. © CC BY 4.0. (c) Self-delamination technique for pattern transfer of thin silicon membranes in liquid media. A graph showing the relationship between the delaminating force per unit length and surface wettability (θ) for films with various degrees of surface porosities (right). Reproduced from [467]. © CC BY 4.0. (d) Demonstration of a thermally released tape-based transfer method (left), enabling precision placement of delicate silicon elements on flexible substrates through programmable laser heating. Optical image of doped SiNMs that were selectively transferred onto a PDMS substrate (right, top) and I-V curves of the fabricated SiNM-based photodetectors showing almost no performance degradation after the transfer process (right, bottom). Reprinted with permission from [137]. © 2020 American Association for the Advancement of Science. (e) Demonstration of a transfer printing process with shape memory polymer-based stamps and controlled laser writing (left). Squared silicon array picked up by a micropatterned shape memory polymer stamp (right, top) and printed onto PDMS elastomeric substrate (right, bottom). Reproduced from [467]. © CC BY 4.0.

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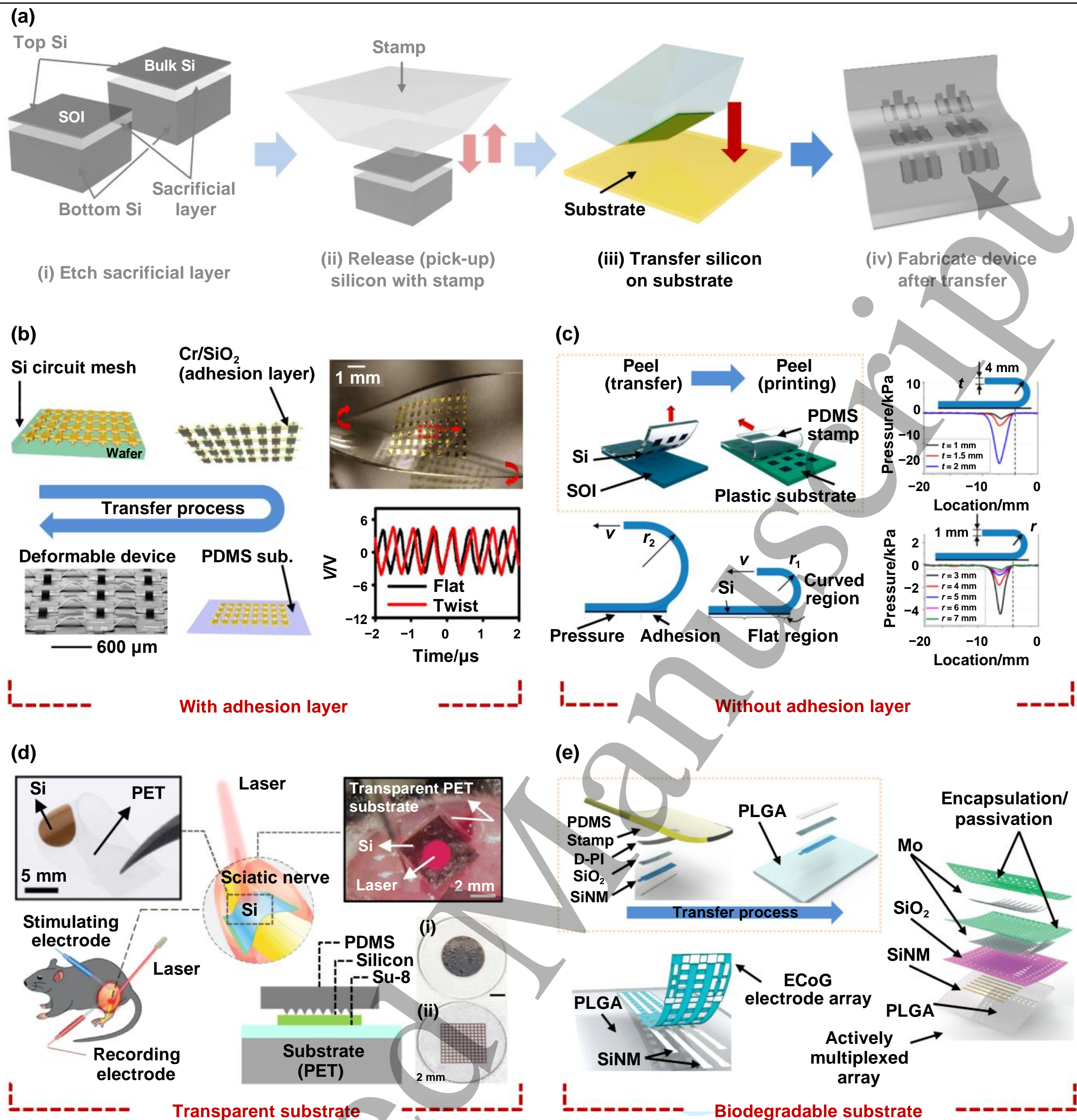

Figure 7. Analysis of various transfer printing techniques for flexible bioelectronics. (a) Schematic of the substrate transfer process for silicon, with only the third step colorized (Step 3: transferring the silicon layer onto the substrate of interest). (b) Demonstration of developing a stretchable electronic circuit utilizing the mesh-structured SiNRs transferred with an adhesion layer of Cr/SiO_2 to maintain the electrical performance under mechanical deformation (left). An optical image of the sample maintaining its physical integrity under significant deformation of twisting (right, top). The graph depicts the unhindered electrical performance of the oscillator, despite the twisting conditions (right, bottom). Reproduced from [482]. © Copyright (2008) National Academy of Sciences. U.S.A (c) Demonstration of an adhesive-free transfer printing method enabled by consecutively peeling off the silicon plates from a SOI wafer and the stamp post-transfer (left, top). Schematic of comparing the induced adhesive (proportional to the curved region) and peeling (proportional to the flat region) forces in two situations in which stamps with different bending radiuses were used. (left, bottom). Two graphs depicting the impact of stamp thickness (right, top) and bending radius (right, bottom) on the pressure distribution during the peeling process of the stamp. Reproduced from [484]. © CC BY 4.0. (d) Transferring silicon p-n diodes onto flexible and transparent PET substrates for optoelectronic neural modulation. Optical images of the transferred device (left, top) with its excellent optical transparency (right, bottom), and the in vivo setup for sciatic nerve stimulation (right, top) are shown. Reprinted with permission from [479]. © 2023 Springer Nature. (e) Transferring SiNMs onto bioresorbable PLGA substrates

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for a transient neural mapping system. Schematics of the fabrication process for transferring the key elements onto a PLGA substrate (left, top), the reported passive electrode array (left, bottom), and actively multiplexed array (right) as a neural electrode for electrophysiological signal monitoring are shown. Reproduced from [485]. © CC BY 4.0.

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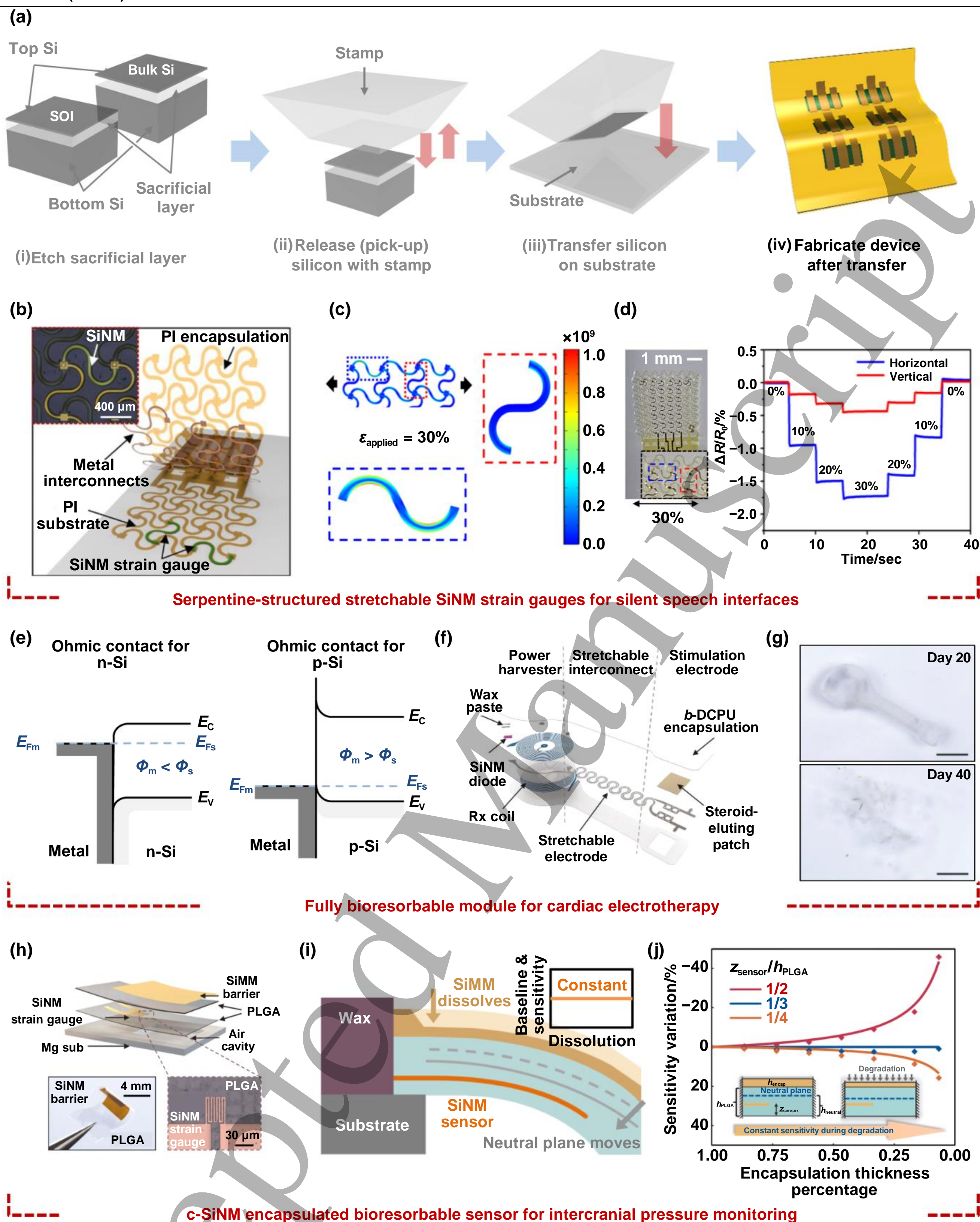

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Figure 8. Analysis of representative flexible manufacturing processes for flexible bioelectronics. (a) Schematic of the substrate transfer process for silicon, with only the fourth step colorized (Step 4: manufacturing the device into its final physical/functional form). (b) Silicon nanomembrane (SiNM)-based stretchable strain sensors with a serpentine structure design for silent speech recognition applications. Magnified image optical showing the SiNM strain gauge as the inset. (c) Design for biaxial strain mapping using a serpentine SiNM structure. (d) Optical image of the sensor and the strain sensing result, highlighting the distinct responses of horizontally and vertically oriented strain sensors under mechanical strain. (b)-(d) Reproduced from [339]. © CC BY 4.0. (e) Schematic of metallization strategies for silicon-based flexible electronics, illustrating the different conditions for metals to be chosen to form Ohmic contacts based on the doping type of the silicon. Energy band diagrams, depicting the band bending results

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of the metal-semiconductor ohmic junction formation for n-type (left) and p-type (right) silicon. (f) Demonstration of paste-based metallization on bioresorbable substrates using a hot-press method to form electrical connections between silicon diodes and stretchable electrodes. (g) Images showing the degradation of a bioresorbable pacemaker at day 20 and day 40. (f) and (g) Reprinted with permission from [121]. © 2022 American Association for the Advancement of Science. (h) Design of a SiNM-based pressure sensor for cardiac monitoring with PLGA encapsulating layers and SiMM barriers. (i) Illustration of the neutral mechanical plane shifting during the dissolution of a SiMM barrier layer, demonstrating how the encapsulation thickness and material location affect the strain gauge's sensitivity. (j) Simulated and analytical results of the relationship between the SiNM strain gauge's position and sensor sensitivity. (h)-(j) Reproduced from [530]. © CC BY 4.0.

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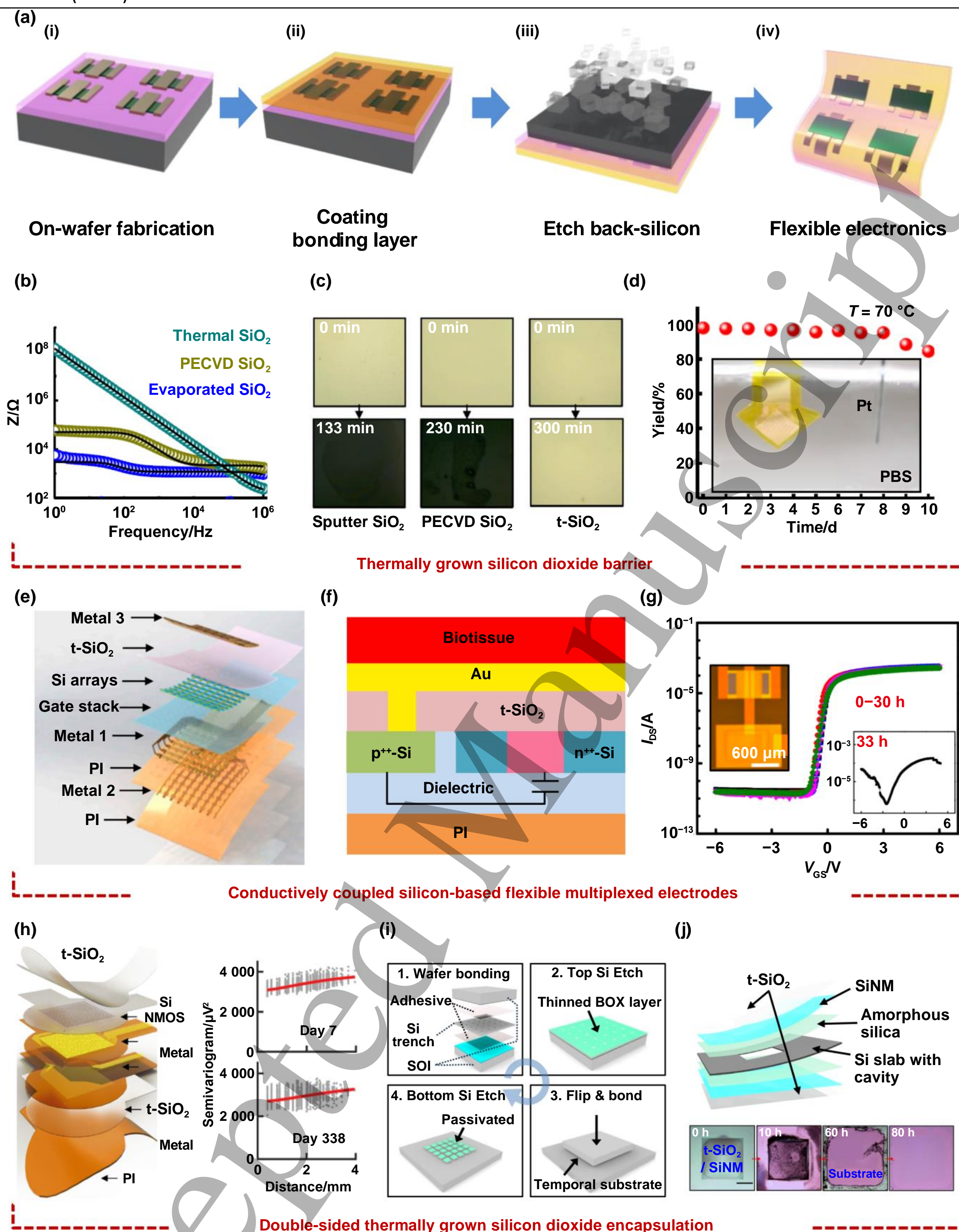

Figure 9. Device transfer technique using backside etching for high-performance encapsulation in flexible bioelectronics. (a) Schematic of the device transfer method, illustrating the full process of the back-etching approach for flexible bioelectronic applications. (b) A resulting log-log plot of EIS analysis between impedance and frequency, as a comparison of SiO_2 layers achieved by different methods. Reproduced from [166]. © CC BY 4.0. (c) Optical images of calcium samples encapsulated with various types of SiO_2 layers, undergoing an electrical calcium test. Only the t-SiO_2 layer at the far right remains unpenetrated after 5 hours. Reprinted with permission from [165]. © 2023 Elsevier Ltd. All rights reserved. (d) Results of an accelerated encapsulation test of a multiplexed array in PBS at 70 °C, demonstrating the stability and high survival rate of the sensing units encapsulated with t-SiO_2 for over 10 days. Reproduced from [166]. © CC BY 4.0. (e) Exploded view of the actively multiplexed array fabricated via back-

etching method, utilizing a t-SiO_2 layer for body fluid encapsulation. (f) Cross-sectional schematic of the fabricated SiNM-based MOSFET encapsulated with t-SiO_2 layer. (g) Accelerated lifetime test results of the encapsulated MOSFET in PBS at 96 °C. The leakage analysis results show stable operations for 30 hours, which scales to 285 days at physiological temperatures. (e)-(g) Reproduced from [187]. © CC BY 4.0. (h) Exploded view of a long-lasting, ultrathin, actively multiplexed electrode array for neural interfacing, with a t-SiO_2 biofluid barrier at both the front and the back side of the device (right). Consistent results of spatial semivariograms of the implanted system between day 7 (left, top) and day 338 (left, bottom) represent the superiority of the t-SiO_2 encapsulation layer. Reprinted with permission from [533]. © 2020 American Association for the Advancement of Science. (i) A generic processing flow of utilizing wafer bonding and backside etching techniques to fabricate a bioresorbable optical sensor for intercranial pressure and temperature monitoring, with a t-SiO_2 biofluid barrier at both the top and the bottom side of the device. (j) Exploded view of the bioresorbable optical sensor with its physical design as a Fabry-Pérot interferometer (top) and optical images of the accelerated dissolution test results in PBS at 95 °C for 80 hours, which scales to 195 days at physiological temperatures (bottom). (i) and (j) Reproduced from [534]. © CC BY 4.0.

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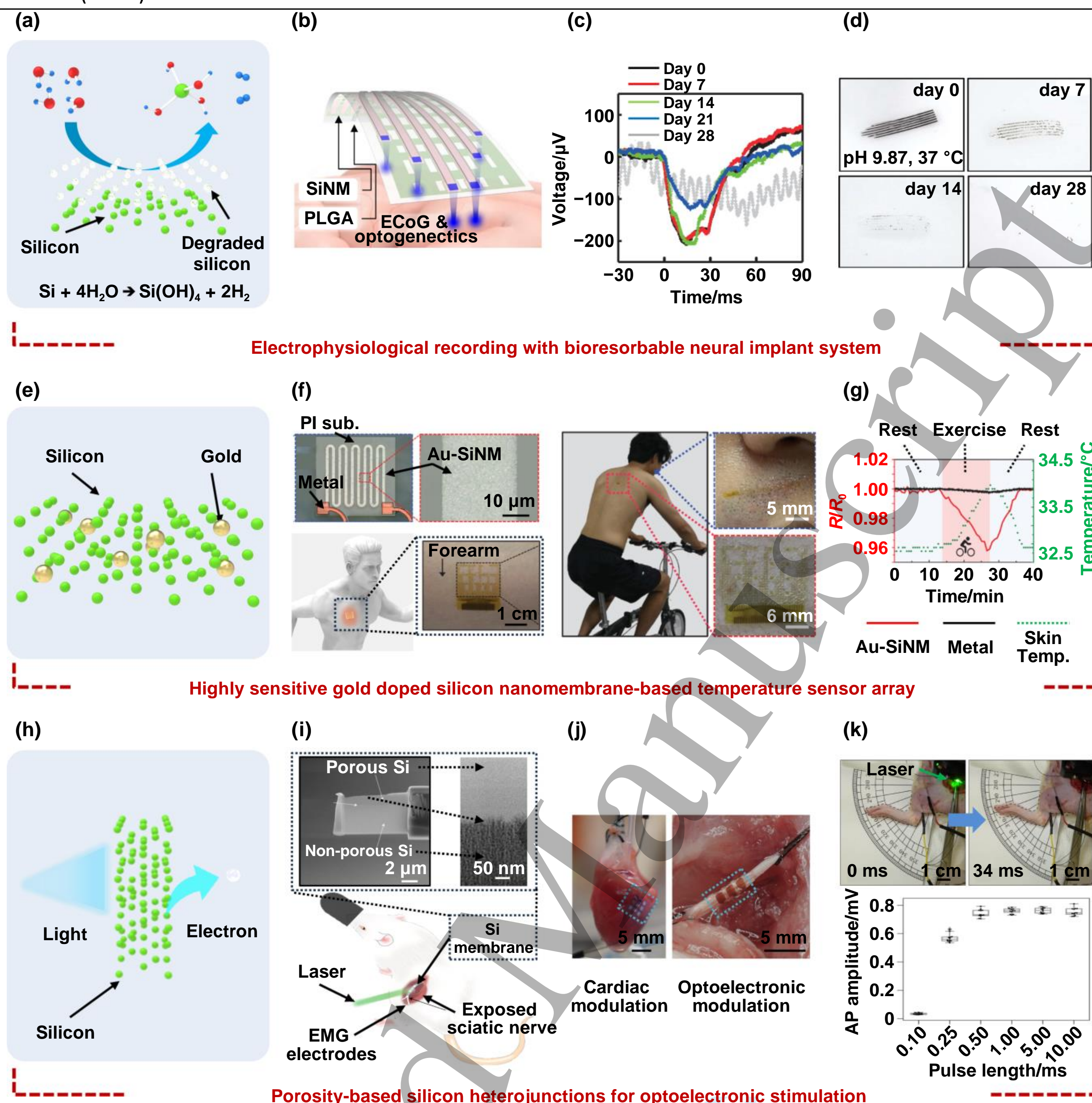

Figure 10. Applications of transfer printed SiNM-based flexible bioelectronics: electrophysiological recording, thermal detecting, and optoelectronic stimulation. (a) Atomic structure illustration of the dissolution mechanism of silicon in bioresorbable implants. (b) Design of a biodegradable neural implant system with integrated Mo/Si electrodes and a flexible PLGA waveguide for optogenetic stimulation and electrophysiological recording. (c) In vivo ECoG recording results of the neural electrode array, showing the optogenetic LFP responses. (d) Dissolution profile of the silicon-based neural system under accelerated dissolution environment of PBS with pH 9.87 at 37 ℃. (b)-(d) Reproduced from [124]. © CC BY 4.0. (e) Atomic structure illustration of the Au-doped silicon. (f) Conformal attachment of the serpentine-structured Au-doped SiNM temperature sensor array to the skin, enabling dynamic and accurate thermal monitoring during exercise. (g) Comparison graph of temperature coefficient of resistance for the Au-doped SiNM and gold. (f) and (g) Reproduced from [352]. © CC BY 4.0. (h) Atomic structure illustration of the photoelectronic stimulation concept. (i) SEM images of the silicon-based porous/non-porous heterojunction and a magnification of the junction interface (top). Schematic of the in vivo setup for photovoltaic sciatic nerve stimulation (bottom). (j) Optical images of the well-adhered device without additional assistants against the left ventricular wall (left) and sciatic nerve (right), according to each purpose. (k) In vivo experiment results showing sciatic nerve stimulation in a rat model (top) and graph of the AP amplitude generated in response to NIR lasers with different pulse lengths (bottom). (i)-(k) Reprinted with permission from [551]. © 2022 Springer Nature.

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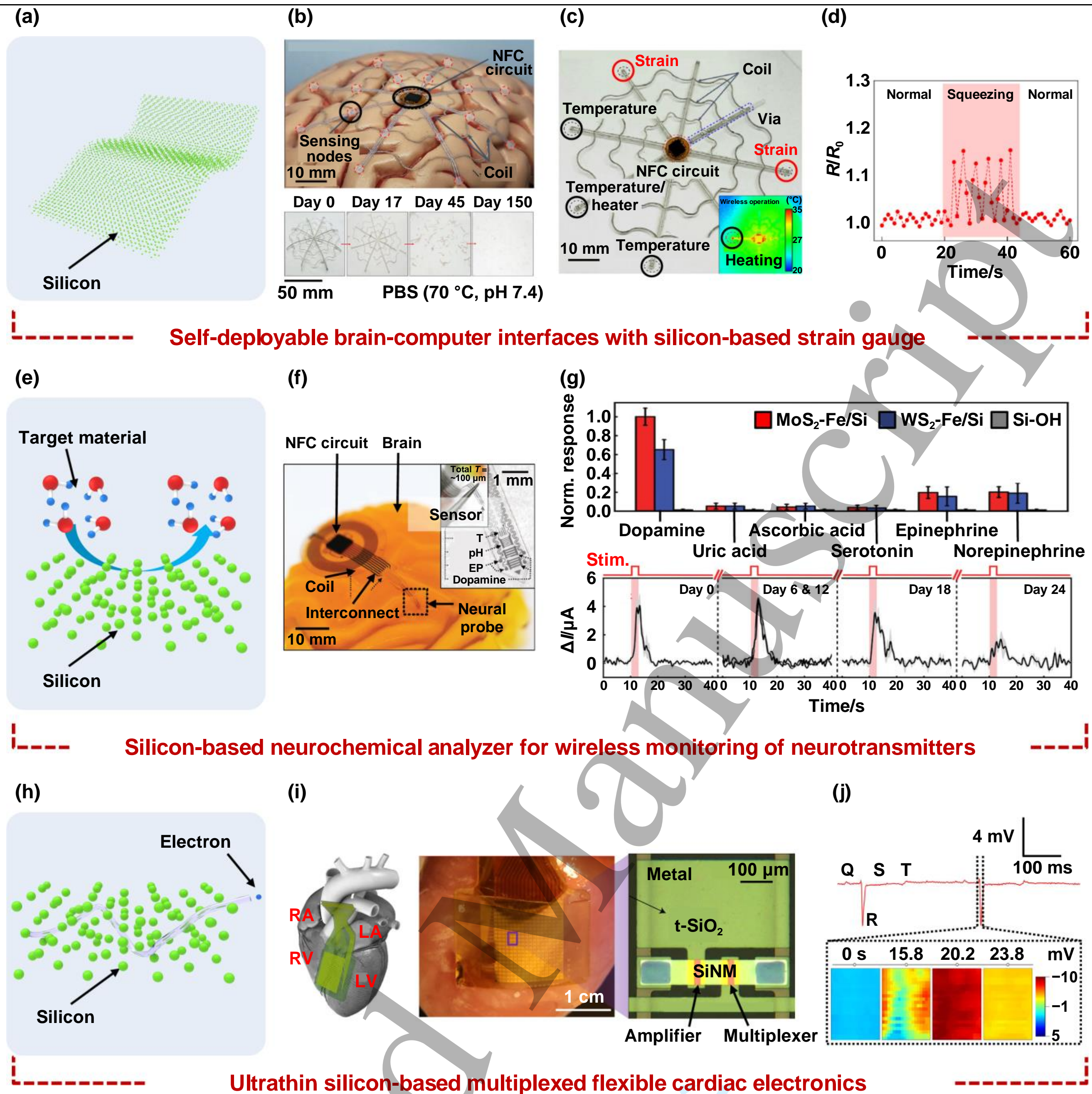

Figure 11. Applications of transfer printed SiNM-based flexible bioelectronics: mechanical monitoring, biochemical sensing, and active device. (a) Atomic structure illustration of the mechanically deformed silicon. (b) Device layout and dissolution profile showing the significant expansion of the self-deployable tent structure after implantation over a large brain cortex area and its dissolution. (c) Integration of silicon-based strain sensors and other functional components in a mesh structure for simultaneous biomechanical signal acquisition. (d) Graph of the strain sensing results induced by abdomen squeezing via the brain-implanted device. (b)-(d) Reprinted with permission from [476]. © 2024 Springer Nature. (e) Atomic structure illustration of the biochemical sensing using silicon. (f) Image of the neurochemical analyzer using selectively doped silicon nanomembranes to enable sensitive MoS_2 and WS_2 detection, with an enlarged view of the heterogeneous system in the inset. (g) Graph showing the enhanced detection sensitivity of the neurochemical analyzer, achieved through the integration of 2D materials to improve neurotransmitter monitoring. (f) and (g) Reprinted with permission from [545] Copyright © 2022 by John Wiley & Sons, Inc. (h) Atomic structure illustration of the high electrical mobility of silicon. (i) The flexible silicon transistor array using capacitive coupling technology and transfer printed t-SiO_2, reducing current leakage during cardiac activity recording. A photograph of the system on a rabbit heart (middle) and an optical image of a single cell (right). (j) Electrocardiogram recording obtained by the voltage trace of a single node (top) and the high-density cardiac electrophysiology mapping results by the SiNM transistor array (bottom). (i) and (j) Reprinted with permission from [162]. © 2017 Springer Nature.

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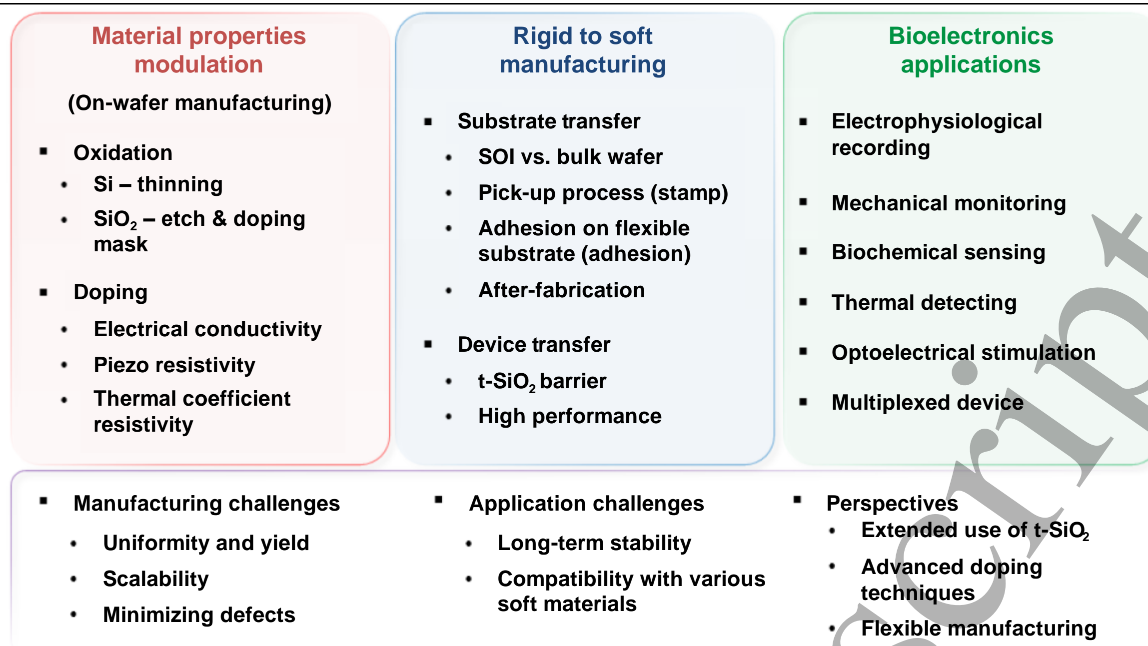

Figure 12. Summary and perspectives of manufacturing of single-crystalline silicon based flexible bioelectronics

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Table 1. Examples of bioelectronic devices categorized by the applied transfer method and their accompanying representative key features.

Type of transfer process	Type of device	Bioelectronic device example	Key features	Ref.
Substrate transfer	Passive	Resistor	Strain sensing, pressure sensing, temperature sensing, electrochemical sensing, photodetection, orientation dependence, doping dependence, bioresorbability	[117–118, 204, 339, 348, 352, 476, 518, 545–550]
		Electrode	Recording, stimulation, bioresorbability	[124, 485, 545, 551–556]
	Active	Diode	Rectification, photovoltaics, photodetection, thermal sensing/actuation, bioresorbability	[81, 115, 121, 137, 289, 479, 508, 552, 557–560]
		Transistor	Amplification, multiplexing, logic and computation, pressure sensing, bioresorbability	[81, 111–112, 173, 476, 552, 561–563]
Device transfer	Passive	Resistor	Pressure sensing, temperature sensing, photodetection, bioresorbability	[172, 548, 550, 564–565]
		Electrode	Recording, stimulation, body fluid barrier, bioresorbability	[186–187, 566–569]
	Active	Diode		
		Transistor	Amplification, multiplexing, pH sensing, gas sensing, humidity sensing	[162, 187, 533, 566, 570]

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